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FINAL REPORT

CYLINDRICAL MAGNETIC THIN FILM MEMORY ELEMENT

August 15, 1962 to November 15, 1962

AN ENGINEERING DESIGN STUDY PERFORMED
FOR
JET PROPULSION LABORATORY
Pasadena, California
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Statement of Work SW-2893, Rev. A

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1.0 SUMMARY

An engineering design study program, August 15, 1962 to November 15, 1962, has been conducted to determine the suitability of using a thin magnetic film plated on a wire substrate in a spacecraft memory system of approximately one million bits. The memory system is for the storage of science instruments command and control program data and as a buffer store for data from the instruments.

The study program was conducted under Jet Propulsion Laboratory Contract No. 950383 and statement of work SW-2893, Revision A. In addition to the measurement of the electrical parameters and performance of the plated wire memory element, the following design considerations were studied:

A. Destructive vs. nondestructive readout.

B. Random vs. sequential access.

C. Data transfer rates.

D. Combinations of magnetic and semiconductor elements.

1.1 Development Status

Measurements made on a number of plated wire samples show:

a. Successful operation of adjacent bits of stored information at a density of 25 bits per inch of wire. Some wire samples were successfully operated at a bit density of 50 per inch.

b. True nondestructive readout of the stored information by application of a magnetic field parallel to the wire (parallel to the hard axis of the magnetic thin film).

c. Simple write-in of new information requires only 20 milliamperes of pulse current in the wire overlapping the readout field.

d. Wire operation is unaffected by temperatures from -50°C to 125°C by actual test.

e. Sensitivity to mechanical stress is practically eliminated by controlling the magnetostriction coefficient.

f. The first uniformity - reproducibility data taken on samples from two days of production show that 30% of forty 12 inch lengths of wire are usable.

1.2 Application Possibilities

The plated wire memory element seems to be well suited for spacecraft applications. Although its high speed is not essential, it permits very low average power operation and requires little energy storage because of the very short duration of the drive elements.

The plated wire memory is best suited for word organized (linear select) operation. The non-destructive operation permits the use of multiple length word groups on each select line. This offsets the fact that a diode or selection means is required on each word line by greatly reducing the number of word lines.

Only a few sense amplifiers and information drivers are needed since each amplifier or driver is gated to one of many bit-sense lines.

This study indicates that using demonstrated techniques and components (not necessarily in volume production) a $1/2 \times 10^6$ bit memory operating at a 100 KC average serial bit rate would have the following characteristics:

a. Average power consumption at maximum bit rate of 260×10^{-3} watts and 240×10^{-3} watts during standby.

b. The size of the memory stack and one level of matrix selection circuitry would be 121 cubic inches. The entire memory system would be 210 cubic inches.

c. The weight of the entire memory system would 9.8 lbs.

One consequence of the high speed capabilities of the memory system is that it is entirely practical to have the memory serve several functions simultaneously. A single buffer can serve both the data output of the instruments and the buffering of accumulated data to the transmitter.

1.3 Future Developments

A small, one year engineering development effort has a very high probability of resulting in a feasibility model to demonstrate the performance set forth in the preceding paragraphs.

In addition, the use of smaller wire for the substrate, which should be investigated, will permit higher bit packing density and lower drive current requirements. The use of integrated circuits in the matrix selection circuits that are incorporated in the memory stack may permit a significant reduction in the volume and weight.

2.0 PRESENTATION OF RESULTS

The technical data presented in this report is a "state-of-the-art" report about the rapidly developing thin magnetic film memory element plated on a wire substrate. Some of the test techniques are not entirely satisfactory since some wire samples show puzzling results. Without any doubt, some of the tests will be significantly modified as will the characteristics of the plated wire by additional development.

2.1 Operation of the Plated Wire Memory Element

The element under study is a beryllium-copper wire, 0.005 inches in diameter with a 12,000 Å layer of copper, and a final layer of nickel-iron (80%-20%) approximately 10,000 Å thick. During the electrodeposition of the nickel-iron, a circumferential magnetic field is generated around the wire to establish an easy axis of magnetization or the anisotropy axis. The hard axis of magnetization is established along the length of the wire (Figure 2.1.1 and 2.1.2). The magnetic anisotropy establishes two stable positions for the magnetization vector. The stored information is read by applying a magnetic field (H_T) perpendicular to the easy axis (See Figure 2.1.1). Opposite polarity signals are induced by the rotation of the magnetization vector from opposite stable states. The location of the information along the length of the wire is determined by the intersection of the magnetic wire and a word line passing orthogonally over the magnetic wire.

When the stored information is read by applying an axial field caused by current in the word line (Figure 2.1.1), the magnetization vector is rotated reversibly through an angle less than 90°. The magnetic wire is coupled only to the flux change along the easy axis and the rotation of the magnetization vector induces a voltage in the wire which may be detected at the ends of the wire. Thus, the magnetic wire also acts as a sense line. Since the rotation is reversible, the magnetization vector returns to its original orientation on the easy axis when the axial field is removed. This results in a non-destructive readout.

Writing is accomplished by applying a small circumferential magnetic field (H_L) caused by a current flowing in the wire. This field is coincident with the trailing edge of the field caused by the word strap and guides the magnetization vector to one of its two stable states depending upon the circumferential field directions.

There are two types of test fixtures which are used to evaluate the plated wires. The first type consists of a hollow glass rod with a short solenoid wound on it. The transverse or read current is applied to this solenoid. Plated wires are inserted into the hollow rod and connections for the write currents and signal outputs are made with pools of mercury. The mercury contacts are approximately one inch apart. By sliding different sections of the wire into the solenoid, the uniformity can be examined. This test device permits a rapdi examination of many wires.

A second device has been constructed to represent a partial memory plane. This device allows the investigation of performance versus various packing densities, the effect of drive line geometry, and also the evaluation of various construction techniques. It consists of a grooved ground plane over which are placed flexible word lines. The connections for the write current and output signal from the wire are made by soldering the wire in place. The read current is applied through the flexible word lines and returns through the grooved ground plane. The write current and the output from the wire also return through the grooved ground plane.

To obtain information relating to uniformity, reproducibility, and feasibility, it is necessary to know how plated wires behave as a function of various parameters such as H_L, H_T, H_c, H_K, (See Figure 2.1.2), skew of the easy axis, dispersion, plating thickness, and geometry of drive lines. There is no convenient way to examine all of these parameters in detail using one type of test. It is convenient, however, to examine several parameters at one time by applying tests which have parametric displays.

Several tests of this nature have been developed and they have been found to be superior to other techniques in some respects. Information relating to skew, relative dispersion, disturb thresholds, output vs. H_L or H_T and uniformity can be obtained quite readily from these parametric tests. A discussion of these tests as well as results obtained is in another part of this section.

In a word organized or linear select memory, the bit or write current, H_L, will pass through a plated wire containing many bits of information. It is necessary that only those bits along the wire that have a transverse or word field applied coincident with the bit field be altered by the combination of the two fields. Also, it is necessary that the bits of information activated by a bit current not concident with a word current remain undisturbed. It is apparent, therefore, that some limit or tolerance must be placed on H_L. If it exceeds H_c, (Figure 2.1.2), it will allow every bit along the wire to be disturbed since switching will occur due to domain wall motion.

A reasonable tolerance to place on the bit current is $\pm$ 20% for the purpose of evaluating the plated wires since a tolerance closer to $\pm$ 5% can be achieved in an acutal memory using conventional techniques. The worst case now becomes that case where H_L minus 20% H_L is used to write and H_L plus 20% H_L is used to disturb or H_L disturb/H_L write = 3/2.

At present, wires can be operated with a nominal bit current of 20 milliamperes. For test purposes, a bit current of 16 milliamperes was used for writing and a bit current of 24 milliamperes was used for disturbing. Upon application of 10^9 disturb pulses, the output was reduced in amplitude less than 10%. See Figure 2.1.3a for pulse test pattern. If a sneak bit current should occur coincident with the word current, disturbing will occur if the sneak current exceeds some threshold. A typical value for allowable sneak current found using the test setup in Figure 2.1.3b is 15% of H_L and has been as high as 20% of H_L on some wires.

The selection of a word current level, H_T, and its tolerance depends on the characteristics of the wire. The normalized effective word field is $\frac{H_T - H_D}{H_K}$ where H_K (Figure 2.1.2) and H_D are the anisotropy field and demagnetizing field of the wire. Based on present drive line configurations and wire characteristics, a word current equivalent to 800 milliampere-turns is required for an NDRO output of 15 millivolts peak with a switching speed of 40 nanoseconds.

When opposite bits of information are stored close together on a plated wire, interaction and domain wall creep must be investigated. Three bits of information were stored on a wire on 40 mil centers. A "one" was first stored in the center position, then a zero was written into the two outside bits simultaneously one billion times while reading only out of the center bit so that the effect upon the amplitude of the center bit could be monitored periodically. See Figure 2.1.4. The output of the center bit decreased 20% after the first writing of the zeroes and remained constant thereafter indicating some interaction and no creeping within the billion writes. It is felt that this 20% reduction in output can be tolerated in order that a packing density of 25 bits per inch be realized. If the packing density were reduced to 20 bits per inch, the interaction would be reduced.

One type of parametric test that has been devised consists of applying a periodically alternating bit current down the wire while applying a constant pulse word current by means of a word strap. See Figure 2.1.5. The repetition rate of the word current is much higher than that of the longitudinal field. The relative frequency of the two fields affects the results in a manner not fully understood. However, high relative frequency ratios give values of write threshold and relative dispersion that are asymptotic and agree with pulse operation of the wire. An X-Y plot of output vs. longitudinal field is displayed on an oscilloscope from which the skew and relative dispersion can be readily observed. (Figure 2.1.5).

The measuring of the absolute dispersion of a plated wire cannot be done with a continuously plated wire but must be done with a discrete section of plating. Using a sectioned wire, a dispersion angle of six degrees was measured at a first attempt. More samples must be measured to reach a sound conclusion. A typical X-Y plot for a plated wire is shown in Figure 2.1.6. The displacement of this curve from the center is indictive of skew. This test is being used as a production line monitor to examine the wires coming out of the plating apparatus. It was found that the wires being plated were skewed due to an external field in the plating cell. This skew can be eliminated by placing the plating cell in the presence of a D.C. field parallel to the wire. A field of approximately 0.08 oersteds reduces the skew close to zero. A trial and error process is being used to cancel the skew exactly.

A slight modification of the above test results in the ability to determine the bit current disturb threshold. The periodically alternating bit current as shown in Figure 2.1.5 is now the envelope of bit current pulses. See Figure 2.1.7. The word current merely probes the state of the average magnetization while the bit current causes the irreversible change in flux which results in X-Y plot shown in Figure 2.1.8.

Fairly good correlation of these tests with operational tests can be reported at this time. It is felt that a direct correlation can be obtained following an improvement in the instrumentation and a better understanding of certain phenomena such as frequency dependency of some wire parameters.

Samples of plated wires were subjected to temperatures between -50°C and +125°C while the parametric tests described above were being performed. No effect due to the temperature could be observed.

Experiments have been performed similar to those described by Figures 2.1.3 and 2.1.4 that indicate a packing density as high as 50 word lines per inch of bit line can be used. A word line width of 10 mils and a space of 10 mils between adjacent bits on the same wire is sufficient to keep the interference between bits at a permissible level. These experiments do not indicate the optimum word line width relative to minimum drive current. If the width of the word line were to be increased, the oersteds per ampere would decrease but the demagnetization field would also decrease. Noting that the effect field "seen" by the wire is the applied field diminished by the demagnetizing field, the effective field strength vs. word line width can be computed. The applied field follows the relationship:

$$\frac{WH}{I} = \frac{0.2}{c}\left[b\left(\tan^{-1}\frac{a-1}{b} - \tan\frac{a+1}{b}\right) + (b+c)\left(\tan^{-1}\frac{a+1}{b+c} - \tan^{-1}\frac{a-1}{b+c}\right) + \frac{1}{2}(a-1)\ln\frac{(a-1)^2+b^2}{(a-1)^2+(b+c)^2} - \frac{1}{2}(a+1)\ln\frac{(a+1)^2+b^2}{(a+1)^2+(b+c)^2}\right]$$

where

W = word line width - centimeters

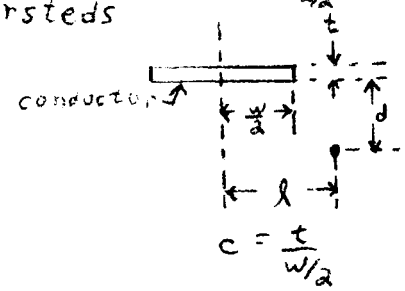
H = magnetic field intensity - oersteds

I = current - amperes

$a = \frac{\ell}{w/2}$

$b = \frac{d}{w/2}$

$c = \frac{t}{w/2}$



where H is the field produced from a single rectangular conductor. The field contribution of a ground plane return is found by using the above equation. A computer was used to solve the equation for various values of a, b and c and the data interpolated to the specific values of interest. To find the optimum word

line width, the current necessary to produce a 90° rotation of the magnetic vector from its rest position was calculated as a function of word line width. The 90° rotation of the magnetization was chosen since the actual operating word drive field will always be less than this amount. For these calculations 90° of rotation was said to occur when the difference of the applied field and the demagnetizing field equals H_K.

$$H_{applied} - H_{demag.} = H_K \text{ for } 90^\circ \text{ rotation}$$

A minimum is expected in these plots since the demagnetizing field is inversely proportional to the length of bit wire that is switched. This value is subtracted from the word drive line sensitivity. The current in the word line required to produce a given field is directly proportional to the drive line width.

Results indicate that a 35 mil word line gives the lowest value of word line drive current. The curves in Figure 2.1.9 show output vs. current required for a 90° rotation. The results to date indicate that a space between words of 15 mils is sufficient and a word line width of 35 mils is optimum, thereby allowing a packing density of 35 mil word lines on 50 mil centers or 20 word lines per inch of bit wire for minimum word readout current.

The test experience has shown that the presence of a transverse disturbing field from adjacent bits is the primary limiting factor on bit packing density along the wire. Reduction of the wire diameter is a simple means to reduce the percent of word drive field that reaches the adjacent bit storage area. Figure 2.1.10 shows the relative field intensity as a function of distance along the wire for two spacings of parallel strip conductors forming the word drive line. Note also that the drive sensitivity in oersted/ampere increases for the smaller wire diameter reducing the required word drive current.

(a) Destructive (Coincident Current) Vs. Non-Destructive Readout (Word Organized)

From a strict logical design viewpoint of a selection matrix, it is obvious that the word organized scheme will require more circuits than the coincident current memory. But when a large memory is viewed from an engineering approach, it is noted that the minimum logical design approach cannot be realized with existing techniques. Some techniques that have to be used in a coincident current ferrite core memory would be to split the sense and inhibit lines which means additional sense amplifiers and inhibit driver circuits. This is normally required so that the half select core output does not become as large as the core output. On a large coincident core memory it is sometimes necessary to drive two selection lines in parallel rather than in series so that the back voltage seen by the driver is not too high. When these practical considerations are taken into account, it can be noted that the coincident current approach would require the same, if not more, circuits than the word organized approach. It is therefore concluded that there is no substantial penalty in weight, size or component count for using the word organized scheme. But now let us mention some of the advantages of the plated wire. Power - since the plated wire can be interrogated with a

narrow current pulse which effectively decreases the average power, low power dissipation is realized. This is shown in the sample memory discussed in section 2.3. Another advantage is, that since it is a non-destructive readout, it is not necessary to re-write the information after it has been read out. This means that the bit or inhibit drivers are not required to be energized except when writing. This saves a substantial amount of power since the power dissipated during the restore cycle is eliminated in the plated wire (non-destructive) approach.

(b) Addressing

It was found while investigating the amount of bits that should be read out in parallel, that the minimum power level will occur when something between five to seventeen bits are read out in parallel. See Figure 2.1.11. Such a condition exists since in the bit serial condition, the word group power becomes the prominent factor while for the fifty bit parallel condition, the power dissipated by the read amplifiers becomes prominent. The increase in power for reading out bit serial would contribute an additional 0.4 watt of power while the fifty bit parallel would increase the power by 0.2 watt. In the sample memory outlined in Section 2.3, a parallel read out of seventeen bits was chosen for its advantage of simple selection and approaching the minimal power level. It was assumed for this calculation that the system would be operating at a word cycle time of 450 usec. It becomes obvious that for slower cycle times or extended inactive periods it would be preferable to use less amplifiers or disconnect D.C. power. A sample calculation is shown on Page 2-16.

(c) Read Rate

Another portion of the investigation covered the effect on power dissipated when increasing the word rate. This is shown in Figure 2.1.12. for a 17 parallel bit read out system. This data indicates that the system discussed can be run at four times the speed with only a slight increase in power. This is obviously desirable since it was indicated for missions in later years the desired program word rate would be increased. Since the plated wire element has no trouble operating at these speeds, no additional circuits are required to increase the speed by a factor of at least ten. The power required to operate the memory at higher speeds will increase, of course, but not proportionally since the standby power is a major portion of the total power. A sample calculation is shown on Page 2-16.

(d) Word Line Selection

A very straightforward method of selecting one of many word lines is to use a simple diode matrix and a number of drivers and switches equal to the square root of the number of word lines. This is the selection method used in the suggested memory systems in Sections 2.3 and 2.4 of this report.

An alternative is the switch core matrix of the type shown in Figure 2.1.13. There is now a switch core for each word group line in place of the diode. The primary windings may now be part of a simple diode matrix, but a more attractive scheme is shown in Figure 2.1.13. In this circuit the switch cores provide both functions of address decoding and word group line selection. This particular method does not involve a D.C. reset bias which is the principle cause of wasted power in other forms of switched core matrices. The design of a large matrix of this type is exacting and a complete assessment of its merits relative to transistor drivers and a diode matrix requires experimental verification.

A second valuable feature of this switching core matrix is that the variation on the output current is much less than some configurations of switch core matrices.

The simplest possible decoding-drive switch core matrix uses a D.C. bias to hold all cores at a bias point such as -3 units of mmf. shown in Figure 2.1.13. Each of the flip flop driver currents is independent and the tolerances that can be maintained on these currents limits the maximum matrix size. In the particular example, the bias current is constrained to be the sum of drive currents from two of the three address flip flops. Thus, switch core number 7 can never exceed zero mmf. regardless of current tolerances. The flip flop driver in the least significant position needs to have reasonable tolerance control since it provides the actual drive pulse and reset pulse.

For a larger matrix, say 256 switch cores, 8 flip flops are needed and 7 of them do not need close tolerance control of the drive current so that the advantages of this type of matrix are more significant. The gating feature eliminates standby power except in the low level flip flops. The use of the independent read and reset driver in the least significant address flip flop means that only these drivers need to have fast rise times. All of the other drivers may be as slow as the cycle time will permit thus saving additional power.

Although a transformer is generally more reliable than a diode, a complete evaluation must consider all of the extra connections and additional costs involved. The temperature dependence and undesirable sneak currents also require a more complete analysis than could be performed at this time.

2.2 Reproducibility and Uniformity

Samples of wires plated during the afternoon of each of two days were collected and cut into lengths of approximately twelve inches. Forty samples were taken. The wires were then examined using the parameter tests described in Section 2.1. Although the number of samples was fairly small, it was felt that it was worthwhile to examine the uniformity of this group.

Each sample was operated under identical conditions and the bit current (information drive current) necessary to write 50% of the saturation output was recorded for the entire length of all wires. The maximum and minimum bit current, expressed as a percent deviation from the average drive required to obtain the specified output was plotted versus the per-cent of wires having the given deviation. The results appear in Figure 2.2.1. The distribution has a peak at 4.8% deviation.

Results of the above tests were then examined to see how many wires would be suitable for use in an actual memory. For a wire to be acceptable, its entire length has to be usable. On this basis, the yeild was 30%.

The definition of usable wires depends upon the disturb threshold and its relationship to the write threshold. Write threshold for a wire length is the maximum bit current needed to write 50% of saturation at any point along the wire. The disturb threshold is the least amount of reversed bit current that causes stored information, at any point along the wire, to diminish to 90%. after many disturb pulses. Therefore, usable wires must all have a maximum write threshold current below, and minimum bit current disturb above threshold one given value of bit current.

Magnetostriction data was also gathered from these samples of wire. The H_k of the wires was measured with a 5 kc B-H apparatus. These measurements were made with and without a tensile stress applied to the wire under test. Past experience with planar films indicate that a first order elimination of magnetostriction is present if H_k does not change when the wire is stressed. The wires had an H_k of 3.0 ± .3 oersteds in the unstressed condition and an $\Delta Hk/H_k$ of 2 to 7% or a ΔH_k from -.06 to + 2.1oersteds when stressed. A maximum of 20 grams is applied to the wire so as not to exceed the elastic limit.

2.3 Command and Program Memory

2.3.1 System Design

In a Data Automation System for a spacecraft and in particular, for the Mariner spacecraft, an advantageous system for generating commands to the various instruments would be the use of a random access, micro-programmed memory. The system described in this report has these features and others. One important feature of the memory is that in-flight alteration of a program or any part of a program is permissible while another program is being executed. This has been accomplished without adding any circuit. A system block design of the memory is shown in Figure 2.3.1. In the design of this system, advantage was taken of the fact that by using the plated wire which has a simple NDRO property and a fast switch time, various circuits could be used for more than one function or words could be read out bit serial rather than bit parallel. A good example of this would be the sharing of the A and B registers that are shown in Figure 2.3.1, or the readout of the instructions by seventeen bit parallel rather than all fifty at once. Another feature is to use a portion of the plated wire memory as a register for temporary storage. This allows one to eliminate the additional electronics for a register.

The basic purpose of the micro-program approach is to generate programs by selecting various sub-programs in varying sequences. For the sample memory we have assumed that the instruction word (tells instrument what to do) will be fifty bits. Let us assume we would like 128 master programs and that these 128 master programs are to be made up by assembling sub-programs out of a list of 500 sub-programs. Let us also assume on the average that there are twenty sub-programs per master program and 20 command instructions per sub-program. To allow for a 50 bit command instruction, 128 master programs and 500 sub-programs we require a memory of 530,096 bits. The proposed memory has 557,056 bits.

Referring to Figure 2.3.2, the memory box is visualized as containing three sections. The first section we will call the "Locator Store". The second section, the "Master Program Store" and the third, the "Sub-Program Store". The "Locator Store" consists of the first 128 words or as many words as the desirable number of master programs. These words are 17 bits long, each one denoting the starting address of a master program. The "Master Program Store" consists of approximately 128 x 20 or 2560 words. These words are also 17 bits long, each one denoting the starting address of a sub-program. The "Sub-Program Store" stores approximately 500 sub-programs (10,000 words). These words are 51 bits long, each one being an instruction for an instrument. With this organization, it is possible to locate a "Master Program" by the content of a "Locator" and then locate a "Sub-Program" by a "Master Program" word.

The Central Control and Synchronizer of the spacecraft will initiate the memory's micro-program by sending a program call signal and a "Locator" address. A "Locator" address consists of seven binary bits. The "Locator" then locates the starting address of a "Master Program". A Master Program is in reality a list of consecutive memory locations which may vary in number, or be 20 locations as in our sample. These 20 locations represent 20 memory words each of which contains 17 bits of information. The memory micro-programming feature will allow sequential examination of these master program words. Each word will direct the memory to the beginning of one of 500 sub-programs. Here again, the sub-programs may vary in length but let us assume they are 60 consequtive 17 bit words. The micro-program will read sequentially the desired sub-program list sending the contents of these locations to the C C & S in 17 bit parallel form. Three words from this list will make up the 50 bit instruction word called for as well as an extra bit for ending a sub-program. Each time the C C & S calls for an "instruction word", three groups of 17 bits are sent from the memory (excluding the 51st bit) to the C C & S. When the last word of the "sub-program" has been read, the memory automatically examines the next word of the master program list, and executes another sub-program. These operational cycles repeat until an ending bit appears in a word of the master program. At this time, the memory is available for another master program.

While the memory is sending command instructions to the instruments, during the time the memory is waiting for the next instruction word request from the C C & S, it is free to accept and write information into the memory. While it is the micro-programming control that sequences through a sub-program or a master program, the memory proper is completely random access. Hence, in-flight alteration of any section of the memory is possible.

2.3.2 Logic Design

To verify the scheme outlined, a flow chart (Figure 2.3.3) was prepared. Examining this in conjunction with Figure 2.3.1 will show that the majority of circuits perform more than one function. The memory address decoder with a slight modification was able to be the decoder for both the A and B register counter (CRA and CRB). One set of read amplifiers could be used to drive either CRA or CRB. The register counters are used both for counting and temporary storage. One significant feature is the use of a part of the memory as a storage register to remember the address of the next master program word.

2.3.2 Summary on Circuits

In this section, the recommended circuit approach is outlined. A summary of the power, and component count is shown in Table 2.3.1. The basic circuits and calculations that were used to achieve these results are found in Section 2.3.5.

	Power	Component Count (not in stack)
Logic Circuits	163.8 mw	2688
Sense Amps	75.5 mw	306
Word Selection	18 mw	768
Sense-Bit Selection	3 mw	186
Circuit Total (Read)	261 mw	3948
Write Driver	2 mw	272
Total (not in stack)	263 mw	4220

Size @ 50 components/cu in = 85 cu in

Weight @ Specific Gravity of 1.5 = 4.3 lbs.

TABLE 2.3.1

The circuits that were selected put a high priority on low power dissipation. Since the plated wire element can operate at high speeds (40 nsec), advantage was taken of this fact. Since the memory would be required to read out on command instruction only every 450 usec, it becomes obvious that a system with pulsed power should be used. This system has only two sections where D.C. power is used. They are the logic gates and the read amplifiers. The logic uses transistor-transistor logic which requires D.C. power. This type of circuit offers extreme low D.C. power capability with compactness and simplicity. It uses only one supply voltage and few components to perform a logical desision. The read amplifier is the other circuit that presently dissipates D.C. power. The first three stages of the amplifier are required to operate Class A due to the small signal output from the plated wire relative to the forward drop of diodes or transistors.

Assuming a packing density of 50 components per cubic inch for 4,220 components gives a volume of 85 cubic inches. The volume is calculated based on the use of conventional type components rather than integrated or microelectronic circuits. This is done because it is felt this would provide for a worst case size estimate. Further, not yet proven reliability of integrated circuits and the present non-availability of low power integrated circuits prevent their use in the immediate future. If at a future time when these two objections are removed, integrated circuits used in the memory will make it all the more compact.

2.3.4 Memory Stack Design

The 557,056 bit memory is arranged so that there will be 1024 word group lines and ~~16~~ 32 words of 17 bits each on each word group line. In this example, word group lines are then divided into four groups of 256 each. Each such group defines a frame. A frame is, essentially, a metallic ground plane (supported on a foamed substructure) which is grooved with 544 channels, 272 channels to a side. The plated wires rest in these grooves and then continue to the next three frames in a manner shown in Figure 2.3.4. Thus, the plated wires thread the entire stack of four frames. Each word group line, however, passes over only the two sides of its respective frame. Each word group line and bit (plated wire) line are matrixed in the stack assembly, with the use of transistors, diodes, and resistors. After matrixing, the number of connections to the memory logic circuitry from the stack assembly is reduced by a factor of twelve. The mechanical assembly of the four frames into the memory stack is accomplished with two magnesium pressure plates and silicone sponge rubber spacers between the interconnected frames, and between the pressure plate and the top and bottom frames (See Figure 2.3.4) In this form, the memory stack assembly is 121 cubic inches and wieghs 5 lbs. In the stack assembly there are 544 transistors, 1088 resistors and 1024 diodes. In the accompanying logic circuitry, the packaging density is 50 components to the cubic inch. This results in 85 cubic inches required for the supporting circuitry. The total volume is 206 cubic inches or 0.12 cubic feet.

2.3.5 Appendix

I. Circuit Requirements for Command and Program Memory

A. Logical Functions

	Inverters	Delay Flops	High Power Amplifiers
Program Control	74	24	14
Memory Control	8	14	8
A Registers and Gates	88		
B Registers and Gates	96		
Write Gates	34		
Information Drivers	50		
	350	38	22

B. Circuits

Sense Amplifiers - 17

Bit Drivers - 17

Word Line Selection Switches - 64

Bit and Sense Matrix Gates 32 x 17 + 17 = 561

Word Group Line Diodes - 1024

II. Logic Circuits

Inverter-Transistor-transistor or modified transistor-transistor logic is proposed. 3V supply and 100 ua per circuit are anticipated, making 0.3 mw per circuit. An inverter circuit probably has six components.

High Power Amplifier-The high power amplifier drives 16 inverter circuits. Assuming a circuit gain of 4, the input to the high power amplifier is then, $\frac{16 \times 0.3}{4} + 0.3 = 1.5$ mw per circuit. Component wise, it is probably equivalent to one inverter.

Delay Flop-The delay flop provides timing control. It is roughly equivalent to two inverters giving 0.6 mw, 12 components per circuit.

III. Sense Amplifiers

4-stage amplifier with the first three stages at 0.5 ma and the output stage normally off. Power per circuit = 0.5 x 3 x 3V = 4.5 mw and 18 components

IV. Word Selection Switches (Fig. 2.3.6 shows a possible circuit configuration)

32 output transistors NPN
32 intermediate " (2 1996) PNP
24 Pre-driver transistors PNP
22 pre-driver transistors NPN
32 diodes
110 resistors
110 capacitors
32 transformers
384
x2
768 Components

in addition 1024 line diodes (in the memory stack)

Power = $\frac{.5 \text{ us} \times 3 \text{ cycles}}{450 \text{ us}}$ x 1a x 12v x 1.5 (efficiency) = 18 mw

Standby Power (due to transistor leakage current)

Word Drivers

$$32 \times \max I_{CBO} @ 25^{\circ}C \times 2^{\frac{T}{10^{\circ}C}} \times \text{Aging Factor} \times \text{Supply Voltage}$$

$$= 32 \times 10^{-8}a \times 2^{3} \times 4 \times 6v = 62 \times 10^{-6} w \quad \text{(negligible)}$$

Word Amplifiers

$$= 46 \times 10^{-8}a \times 2^{3} \times 4 \times 3v = 44 \times 10^{-6}w \quad \text{(negligible)}$$

TOTAL WORD SELECTION STANDBY POWER = $2x (62+44) 10^{-6} = 212 \times 10^{-6}$w (negligible)

V. Bit-Sense Selection Matrix

32 PNP pre-driver transistors
22 NPN pre-driver transistors
32 Diodes
100 Resistors
186 Components

also 608 gate transistors } in stack
1216 gate resistors }

Power = $\frac{1.0 \text{ us} \times 3 \text{ cycles}}{450 \text{ us}}$ x 3 ma x 3v x 34 circuits x 1.5 (efficiency) = 3 mw

VI. Write-Drivers

2 NPN transistors
2 PNP transistors
2 Diodes
10 Resistors
16 Components

Power = $\frac{1.0 \text{ us}}{450 \text{ us}}$ x 3v x 20 ma = 0.13 mw circuit

2.4 Buffer Memory

2.4.1 System and Logic Design

A buffer memory using the plated wire as the memory element is proposed. The buffer receives data from the scientific instruments and dumps blocks of data into the tape unit or presents the data to the transmitters. The size of the buffer memory is determined by the data input rates, data output rates, tape reader speed and memory cycle times.

From the description of the command memory, the memory access time is 1.5 us. This time is short enough compared to the input and output rates required of the buffer that interlacing of input and output is permissible and a single memory is sufficient. Furthermore, writing into and reading out of the memory are done in bit serial form, thus not only minimizing the number of read amplifiers and information drivers, but also minimizing the overall power requirement. This last is true because the average operating rate of the memory is so low (set by the data rate from the instruments) that the standby power of one read amplifier exceeds the interrogation drive power. (See Section 2.4.2 for power calculations.)

Assuming it takes 25 ms to start the tape unit, and assuming the highest speed of the tape is 80 thousand bit/second, a wasteful period equivalent to 2000 bits results every time the tape is energized. If a 99% efficiency is desired, then the buffer capacity should be 200,000 bits. If the above assumptions should be changed, the size of the memory would be correspondingly different. The organization of the memory, however, would be essentially the same with the size, power, weight, and circuit count correspondingly modified.

Referring to Fig. 2.4.1, data from the scientific instruments may be sent to the Input Register word serial bit parallel at a rate determined by the sampling rate of the instruments, 8 words/second peak. A 16 bit word is shown here as an example. The data is written into the memory in bit serial form, a word at a time. When the memory is filled, a read-write tape order is initiated. The data is then read out of the memory into the Output Register in bit serial form. If an 8 bit parallel tape unit is used, the Output Register is an 8-bit register. When the Output Register is filled, the character is read into the tape unit. At the top speed of the tape, the memory can be emptied in about 3 seconds. Since the tape speed is much slower than the memory speed, writing into the memory can be uninterrupted when reading into the tape. In this design we have assumed that data can be written synchronously from the tape to the transmitter. If this is not the case, with a slight modification of the control circuitry, information can be written from the tape into the buffer memory. As is also shown in Figure 2.4.1, at an order from the CC & S unit, data can be transferred from the buffer memory into the transmitter. It is suggested 8 bits of data be transferred in parallel into a shift register in the transimitter. Using this method the memory will not be tied up by the slow rate of the transmitter.

Taking advantage of the simple NDRO property of the plated wire element, the memory is to be organized in 1024 words x 256 bits. A diode matrix would be used to select the word lines and a transistor gate matrix for the bit lines. These matrices would be the same types as those described in the command memory.

Fig. 2.4.2 shows the buffer memory in finer logical blocks and Fig. 2.4.3 shows a logical flow chart. Table 2.4.1 lists the circuit requirements of the memory.

TABLE 2.4.1
CIRCUIT REQUIREMENTS FOR BUFFER MEMORY

		Quantity
I.	Logical Functions	
	A. Inverters	268
	B. Delay Flops	27
	C. High Power Amplifiers	12
II.	Circuits	
	A. Sense Amplifier	1
	B. Bit Driver	1
	C. Word Line Selection Switches	64
	D. Bit and Sense Matrix Gates	272
III.	Miscellaneous	
	A. Word Line Selection Diodes	1024

2.4.2 Estimated Power Requirement

The highest read repetition rate at which the memory will operate is 80 kcps at tape read time. It is, however, for at most about 3 seconds in every half hour. The highest average read rate is equal to the highest write rate. This is 8 words/sec x 16 bits or 128 bits/sec. The power requirement is hence estimated for 3 conditions; namely, (1) standby, (2) average power over a long period, and (3) short term power (corresponding to 80 kcps).

1. Standby power

Logic circuits (268 inverters + 27 delay flops x 2)		97.2 mw
12 HPA x 1.5 mw		18 mw
Sense Amplifier 4 stages x 3v x 1 ma		12 ma
	TOTAL	127.2 mw

2. Average Power over a long period

Word driver 1a x 12v x $\frac{0.1 \text{ us}}{4 \text{ ms}}$ x 1.5 (efficiency)		0.45 mw
Bit-Sense Matrix Gate 17 ckts x 3 ma x 3v x $\frac{1 \text{ us}}{4 \text{ ms}}$		0.04 mw
Bit Driver 20 ma x 3v x $\frac{0.5 \text{ us}}{4 \text{ ms}}$		0.004 mw
Logic circuit		115.2 mw
Sense Amplifier		12 mw
	TOTAL	127.7 mw

3. Short term power

Word Driver 1a x 12 v x 1.5 x $\frac{0.1 \text{ us}}{12.5 \text{ us}}$		144 mw
Bit sense matrix 17 ckts x 3 ma x 3v x $\frac{1 \text{ us}}{12.5 \text{ us}}$		12.2 mw
Logic circuit		115.2 mw
Sense Amplifier		12 mw
	TOTAL	283.4 mw

2.4.3 Estimated Size and Weight

Basing our estimates on those obtained for the command and program memory, the size and weight of the Buffer Memory should be approximately 145 cubic inches and 7.3 pounds, respectively.

Sample Calculations of Power vs. No. of Bits Read in Parallel

(Figure 2.1.11 - Section 2.1)

For these calculations it was assumed that a complete program must be circulated within one eighth second and that a typical program consists of 256 words. Therefore, this means that an instruction must be read every 488μsec.

It was then found that the power could be expressed by the following equation:

P_{TOTAL} = Power(fixed) + P(word-amplifiers) + P (word-drivers) +

P(sense-matrix) + number sense amp x P (single sense amp) for a 17 bit parallel read out the power is;

$$= 192.3 + \frac{t_1}{\tau}(723) + \frac{t_2}{\tau}(11,100) + \frac{t_3}{\tau}(1333) + 17\left(\frac{104}{17}\right)$$

Assume: $t_1 = t_3 = 1.5\mu$sec x cycles

$t_2 = 0.15\ \mu$s. x cycles

Instruction rate = 450μsec. = τ

where cycles are the number of pulses necessary to interrogate the memory to read out fifty bits.

$$P_{TOTAL} = 192.3 + \frac{t_1}{\tau}(2,056) + \frac{t_2}{\tau}(11,100) + 104$$

$$= 192.3 + \frac{(1.5 \times 3)}{450}(2,056) + \frac{(.15 \times 3)}{450}(11,100) + 104 = 323 \text{ mw}$$

Sample Calculations of Power vs. Instruction Rate (Figure 2.1.12-Sec. 2.1)

The plot of total power vs instruction rate was made for the system using 17 bit parallel read out. The same basic equation was used that was used for power vs. number of bits read in parallel.

P_{TOTAL} = Power (Fixed) + P(word amp) + P(Word Drivers) + P(sense matrix) + P(Sense amps)

$$P_{TOTAL} = 192.3 + \frac{t_1}{\tau}(2,056) + \frac{t_2}{\tau}(11,100) + 104$$

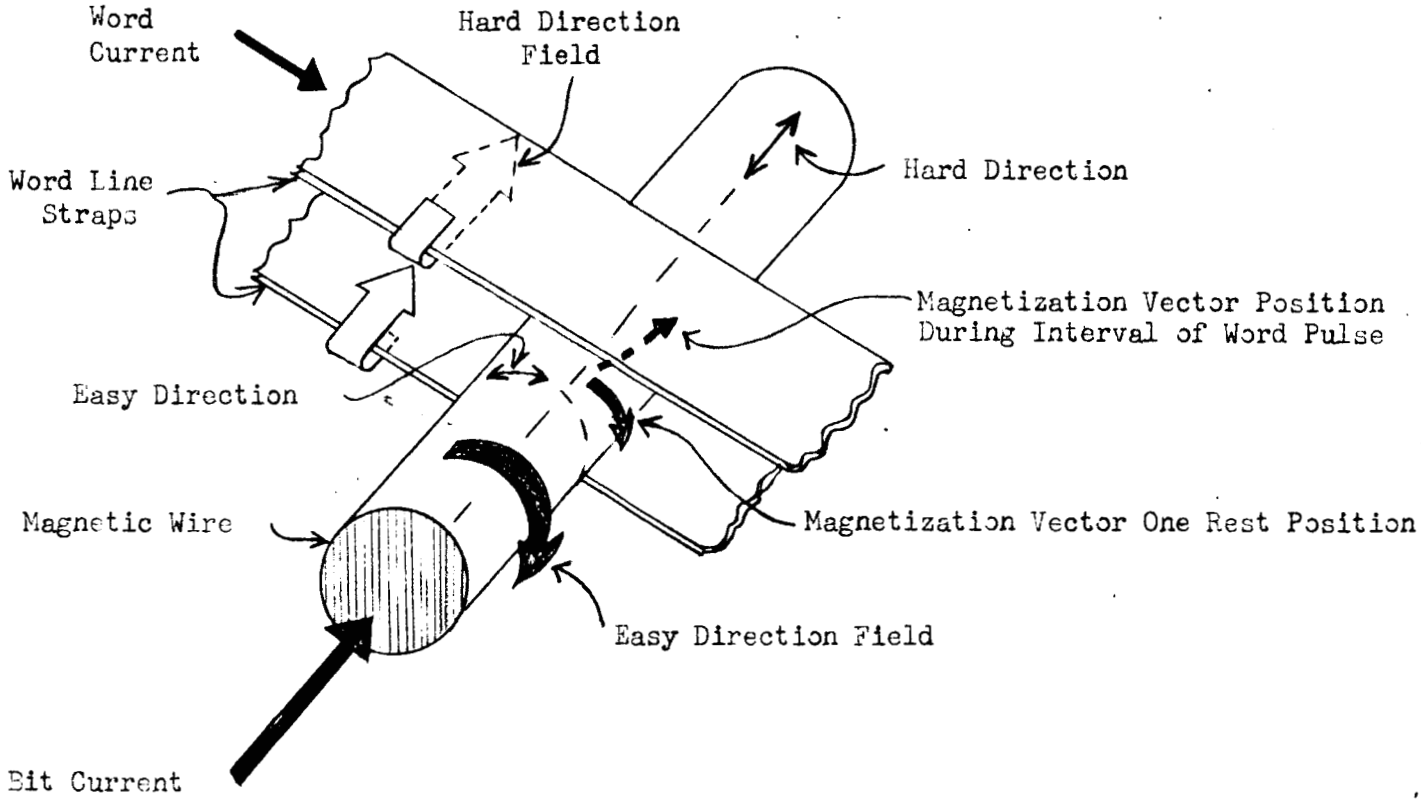
Assume t_1 = 1.5μsec x cycles

where cycles = 3 cycles to read out an instruction

t_2 = variable instruction rate

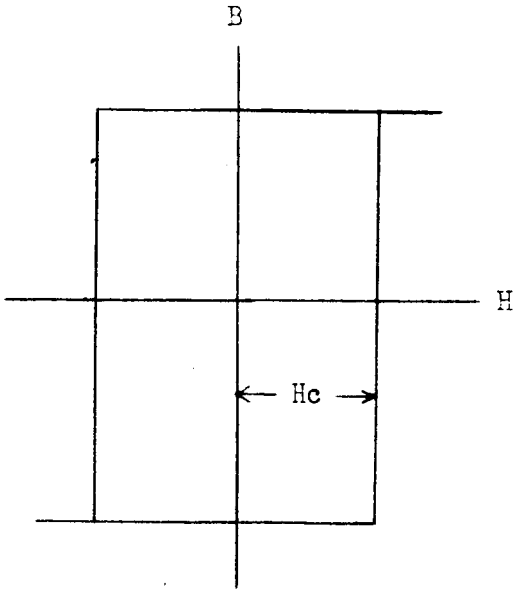
$$P_{TOTAL} = 192.3 + \frac{(1.5 \times 3)}{450}(2,056) + \frac{(0.15 \times 3)}{450}(11,100) + 104$$

P_{TOTAL} = 323 mw

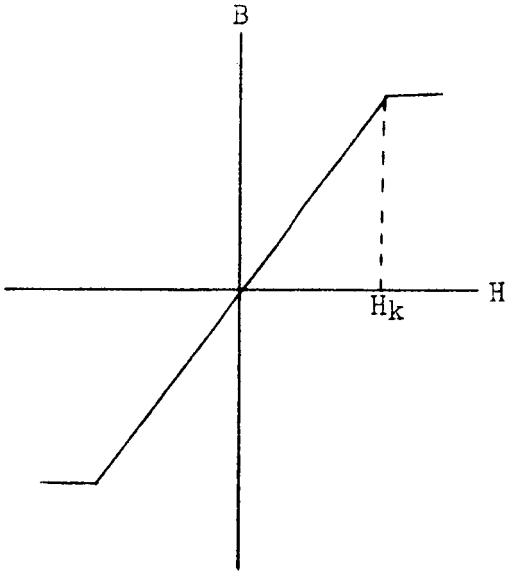


MAGNETIZATION VECTOR POSITIONS DURING READ OR WRITE

FIGURE 2.1.1



Easy Direction Hysteresis Loop



Hard Direction Hysteresis Loop

B-H CHARACTERISTICS OF PLATED WIRE

FIGURE 2.1.2

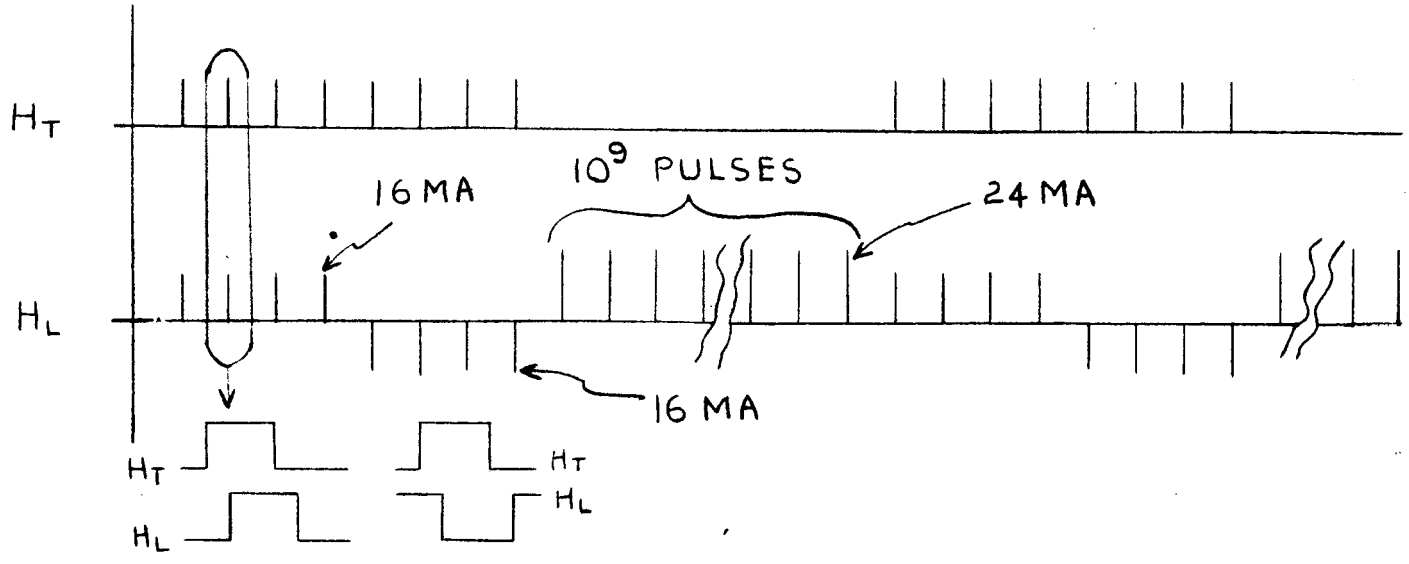


Figure 2.1.3 a

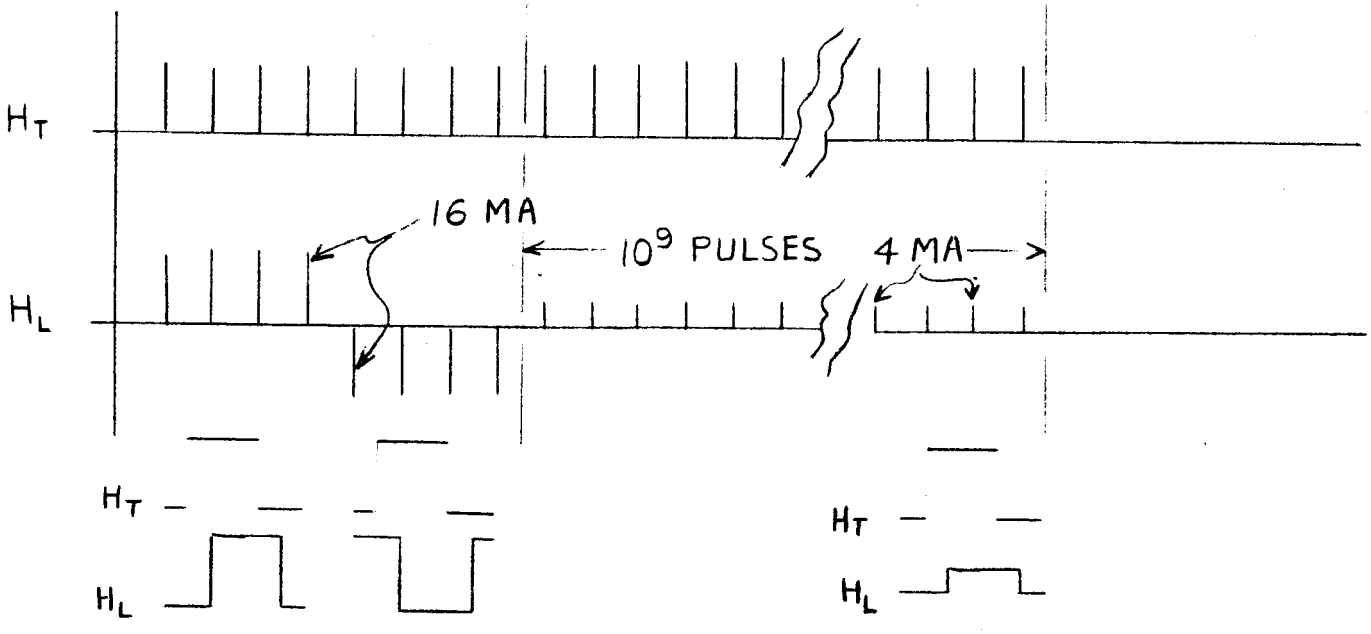


Figure 2.1.3 b

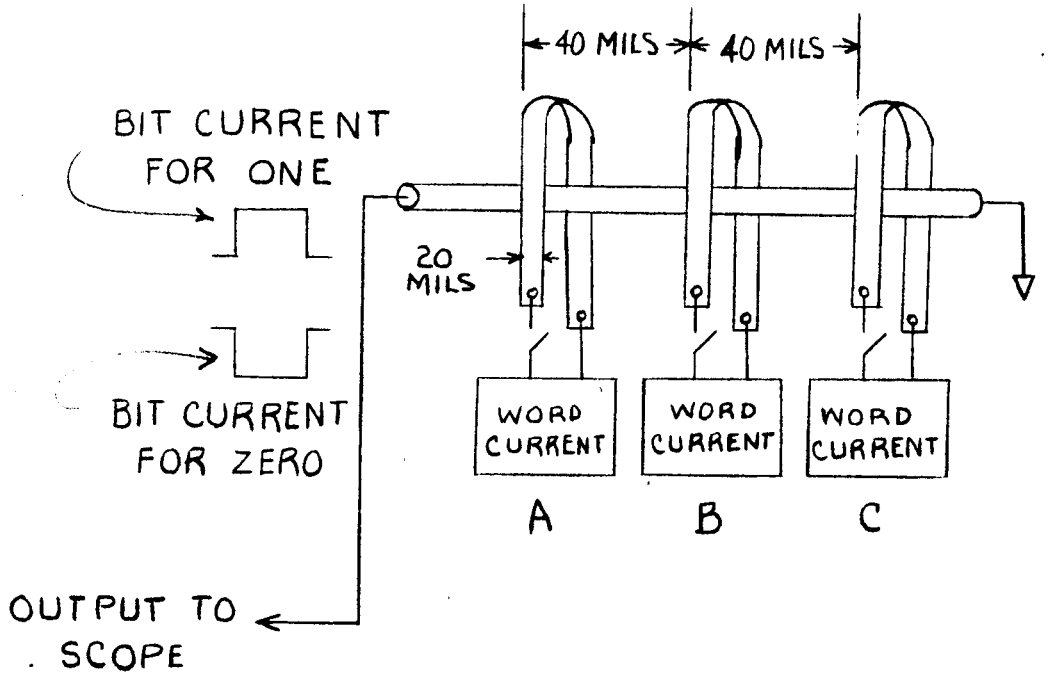

40 MILS
40 MILS
BIT CURRENT FOR ONE
20 MILS
BIT CURRENT FOR ZERO
WORD CURRENT
WORD CURRENT
WORD CURRENT
A
B
C
OUTPUT TO SCOPE

Figure 2.1.4

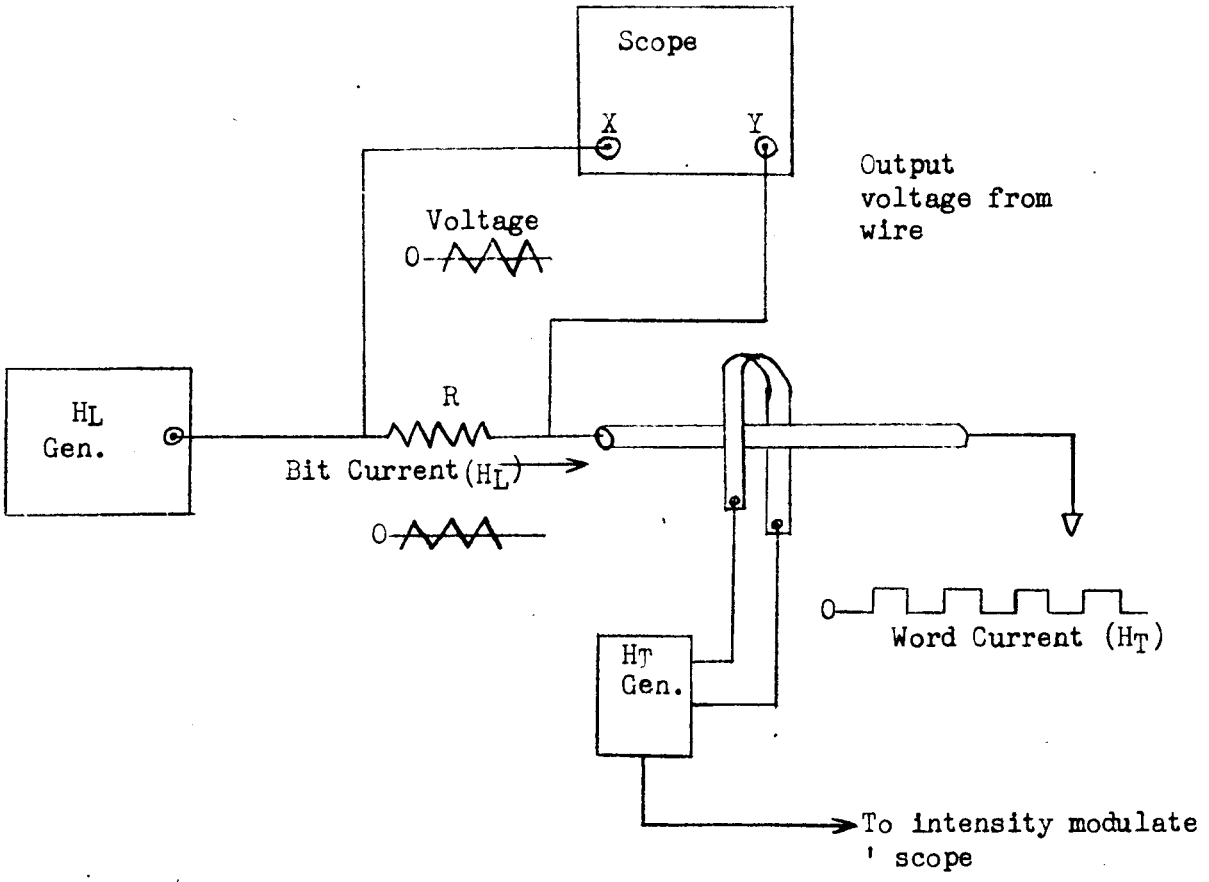


Figure 2.1.5

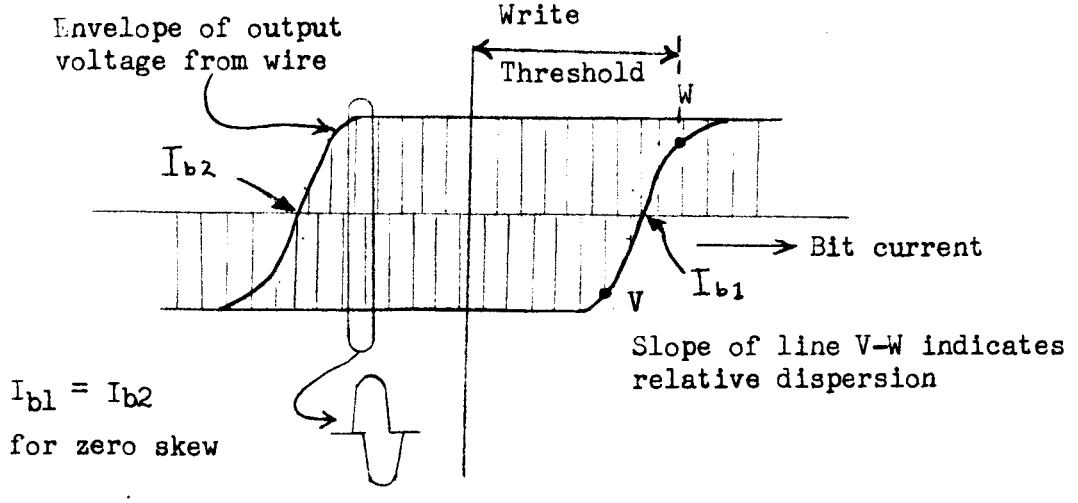


Figure 2.1.6

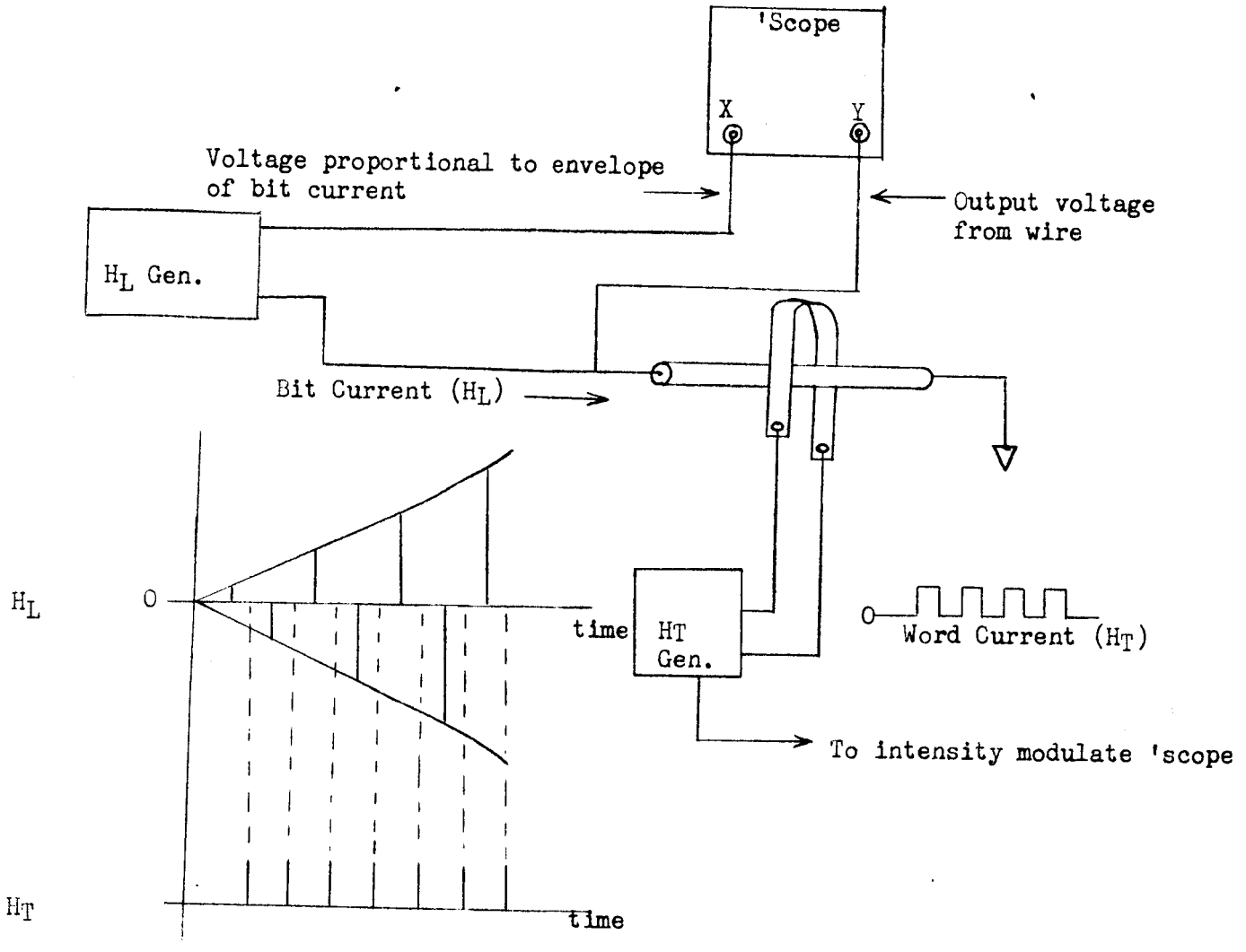


Figure 2.1.7

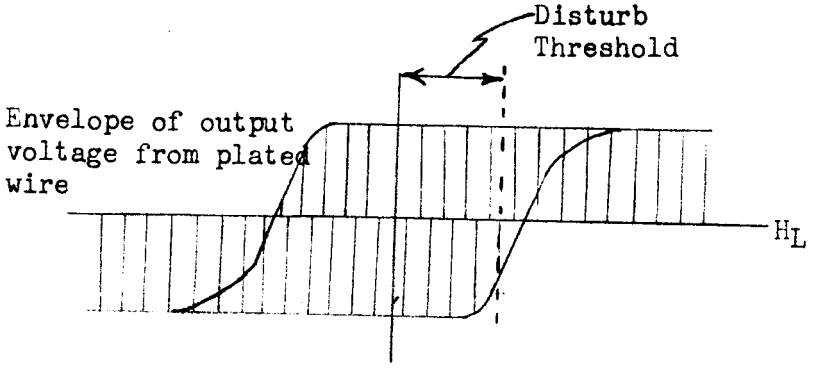


Figure 2.1.8

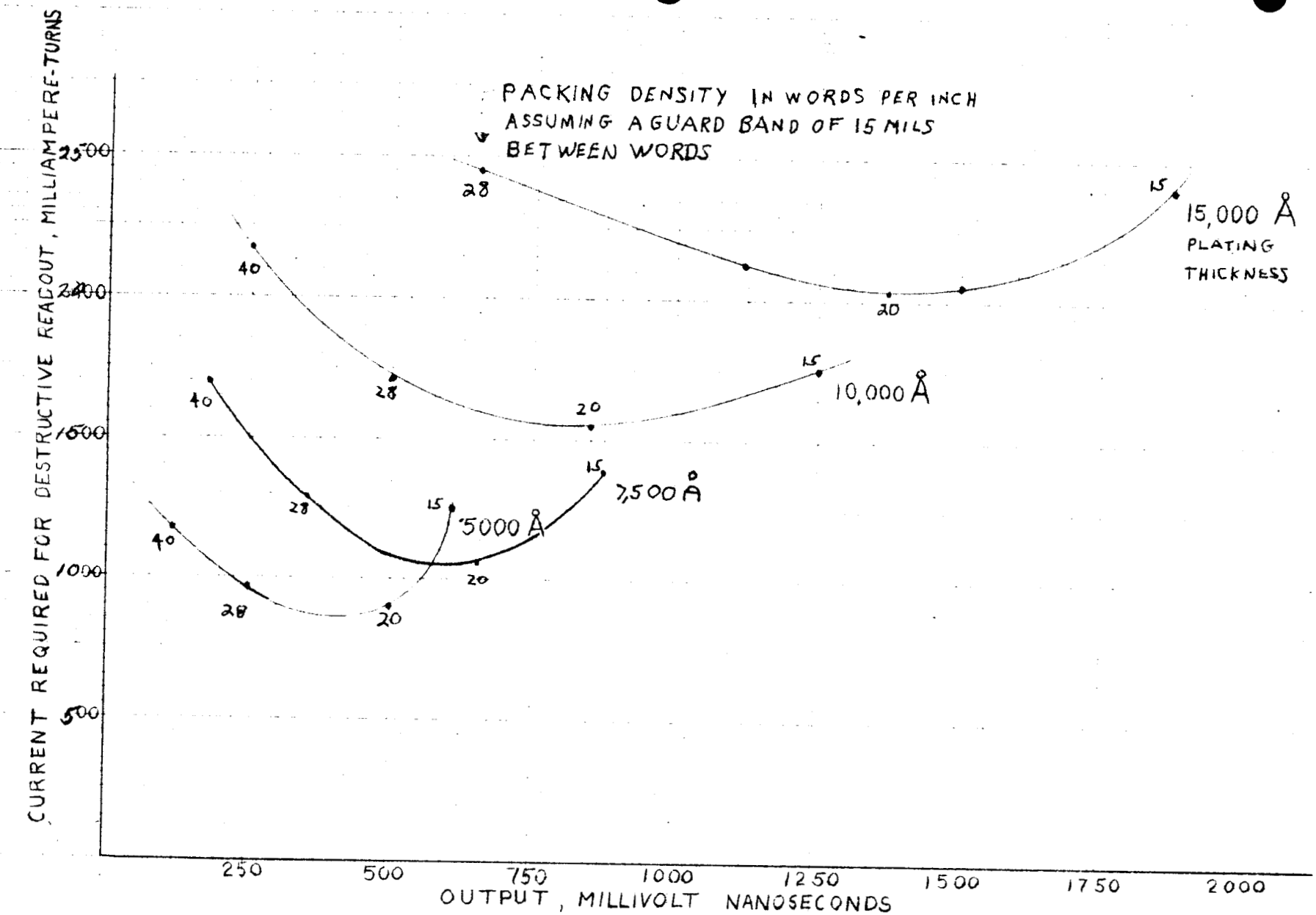

PACKING DENSITY IN WORDS PER INCH
ASSUMING A GUARD BAND OF 15 MILS
BETWEEN WORDS
28
40
20
15
15,000 Å
PLATING
THICKNESS
28
40
20
15
10,000 Å
28
40
20
15
7,500 Å
28
40
20
15
5000 Å
CURRENT REQUIRED FOR DESTRUCTIVE READOUT, MILLIAMPERE-TURNS
2500
2000
1500
1000
500
250
500
750
1000
1250
1500
1750
2000
OUTPUT, MILLIVOLT NANOSECONDS

Figure 2.1.9

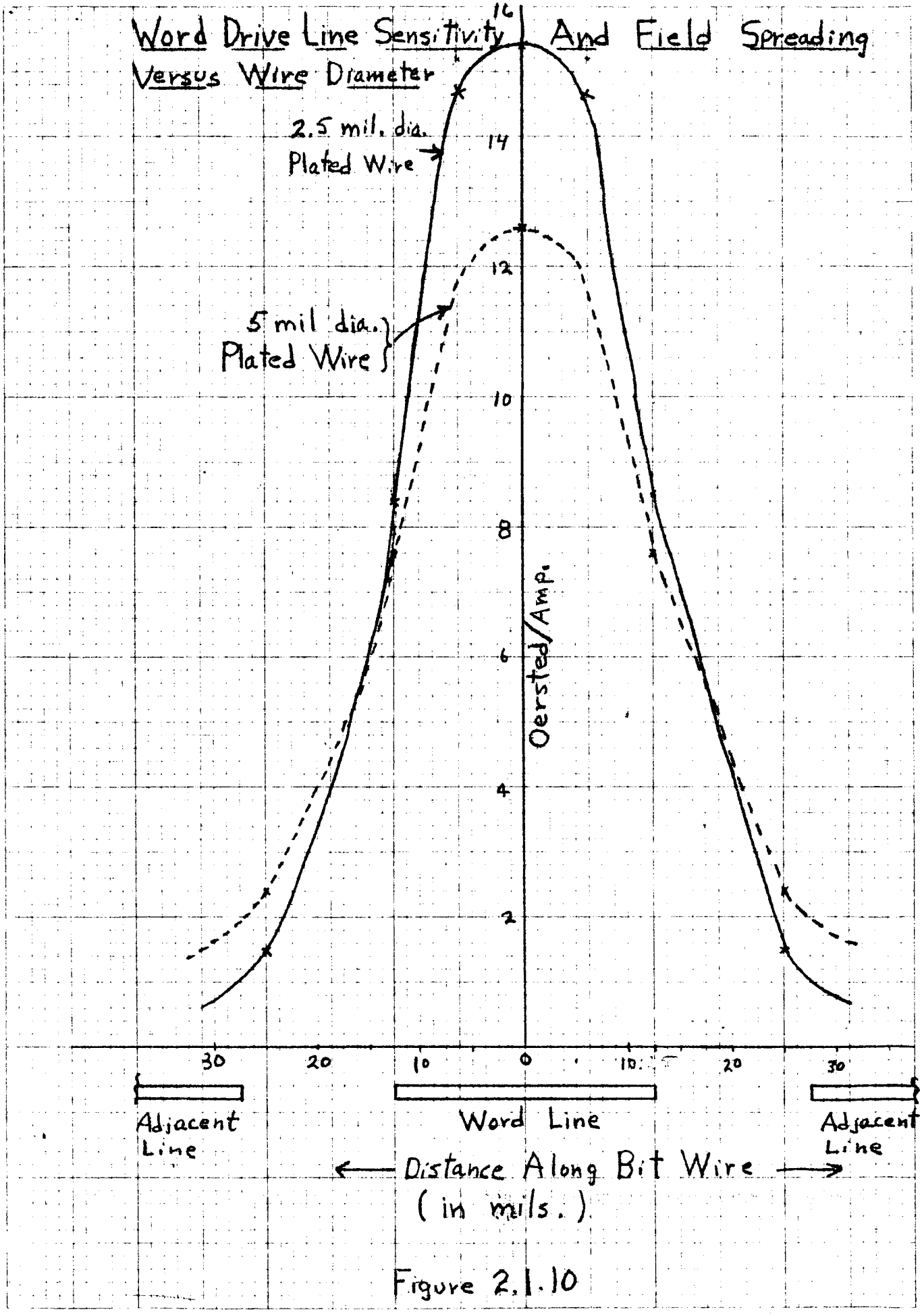


Figure 2.1.10

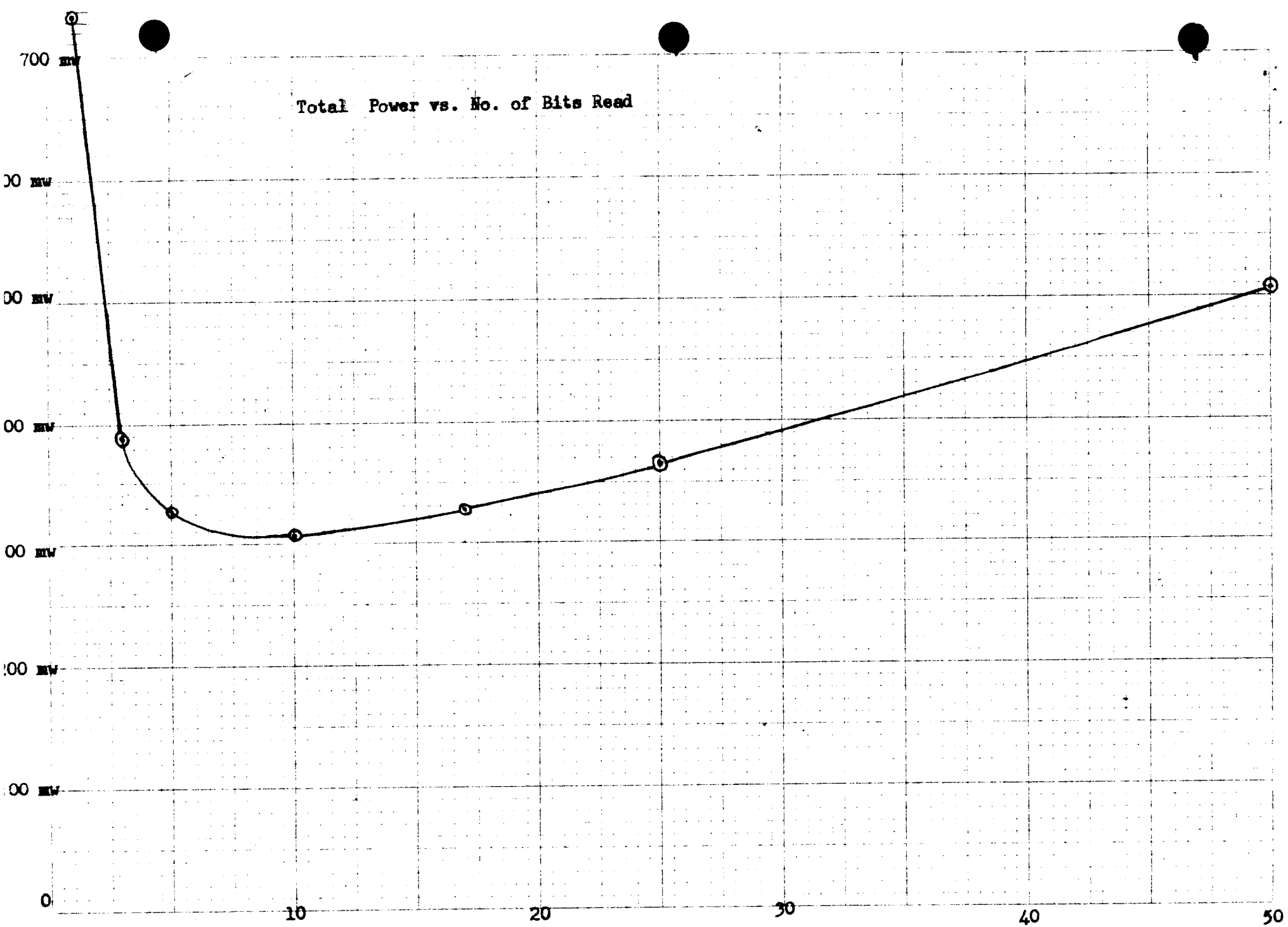


FIGURE 2.1.11

VS.

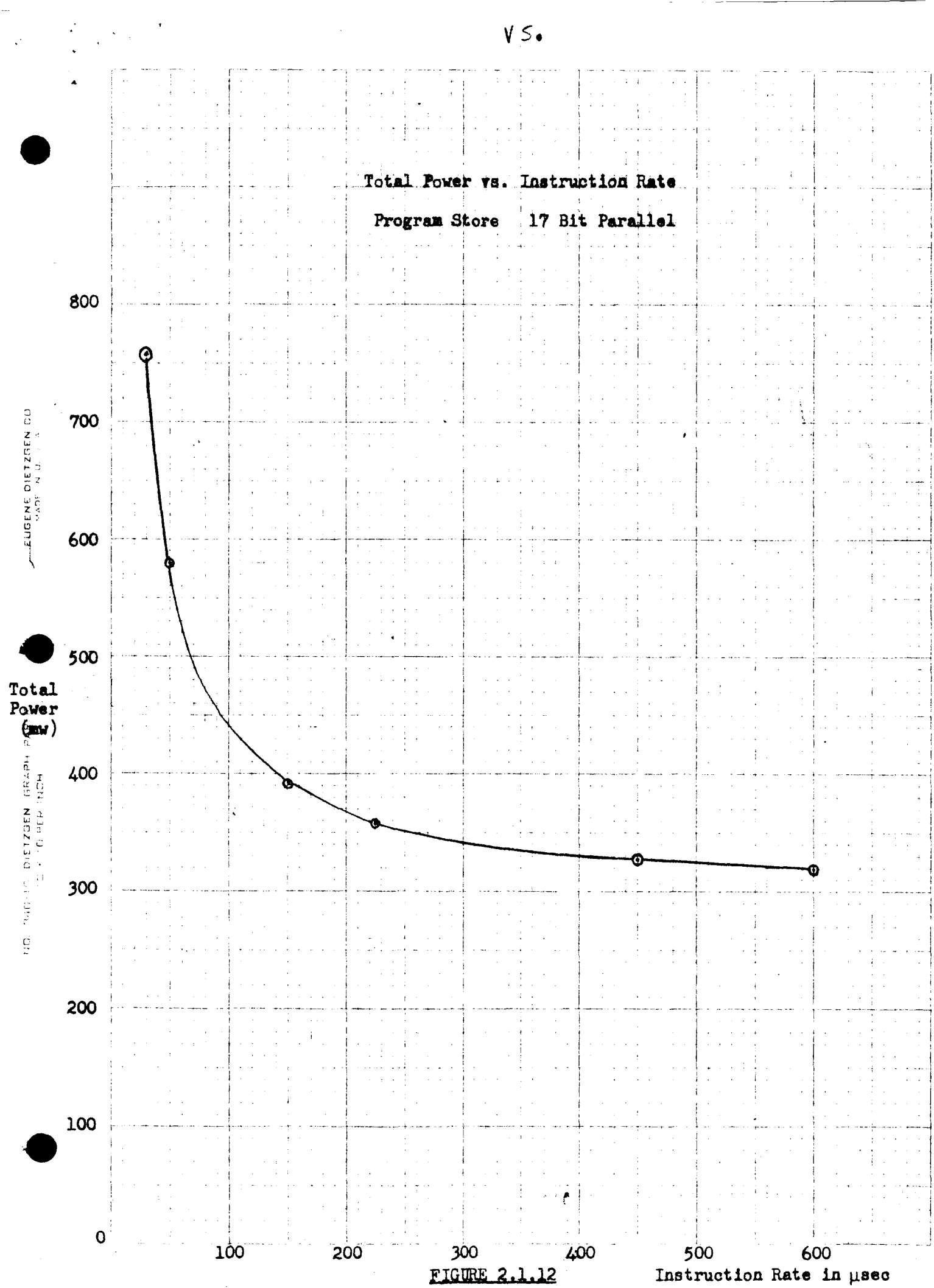


FIGURE 2.1.12

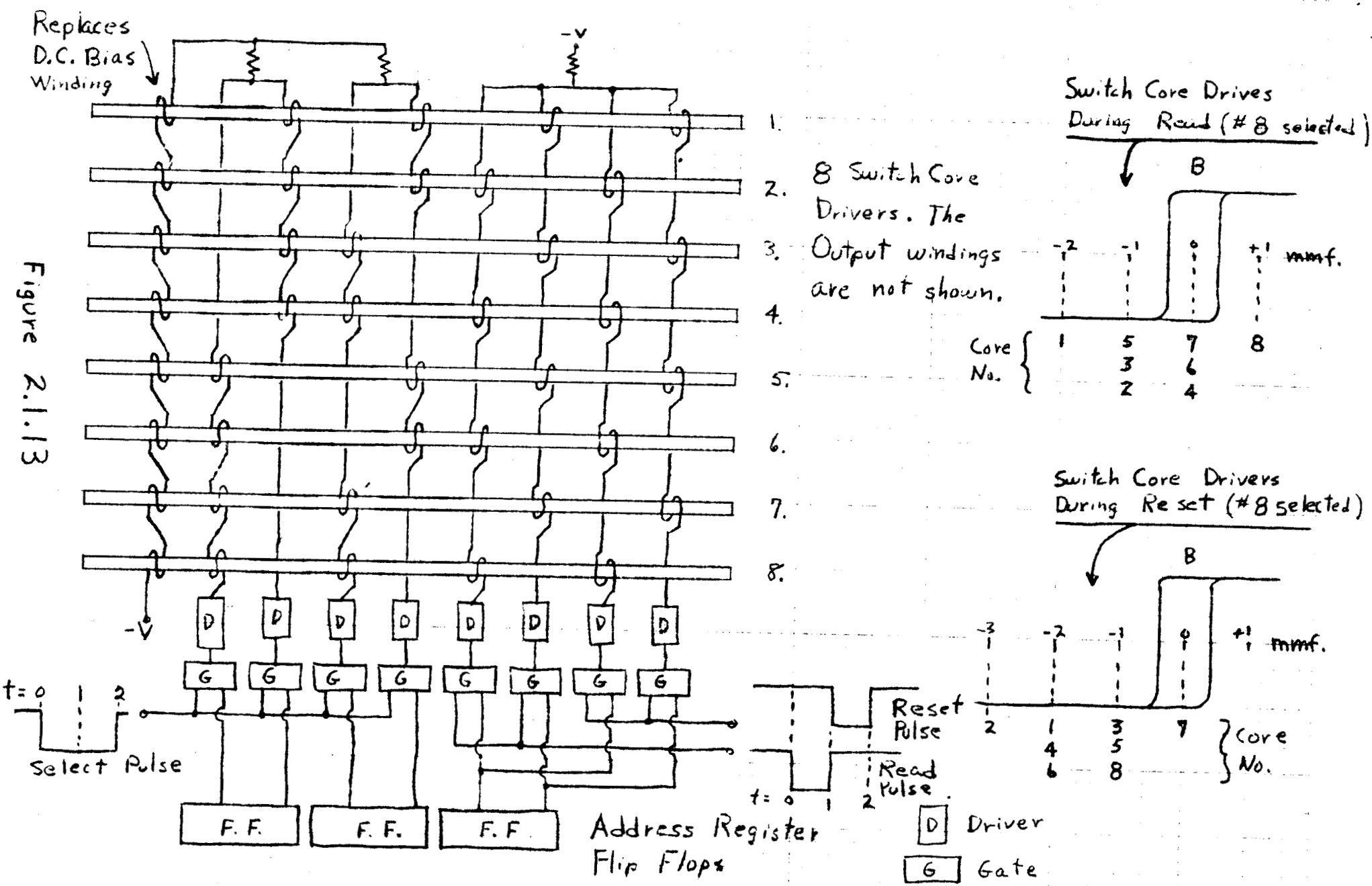

Replaces D.C. Bias Winding
-V
1.
2.
3.
4.
5.
6.
7.
8.
8 Switch Core Drivers. The Output windings are not shown.
-V
D
G
t= 0 1 2
Select Pulse
F. F.
F. F.
F. F
Address Register Flip Flops
Reset Pulse
Read Pulse
t= 0 1 2
D Driver
G Gate
Switch Core Drives During Read (#8 selected)
B
-2 -1 0 +1 mmf.
Core No.
1 5 7 8
3 6
2 4
Switch Core Drivers During Reset (#8 selected)
B
-3 -2 -1 0 +1 mmf.
2 1 3 7
4 5
6 8
Core No.

Figure 2.1.13

Deviation (per cent of average) of maximum and minimum write threshold along forty 12 inch lengths of plated wire

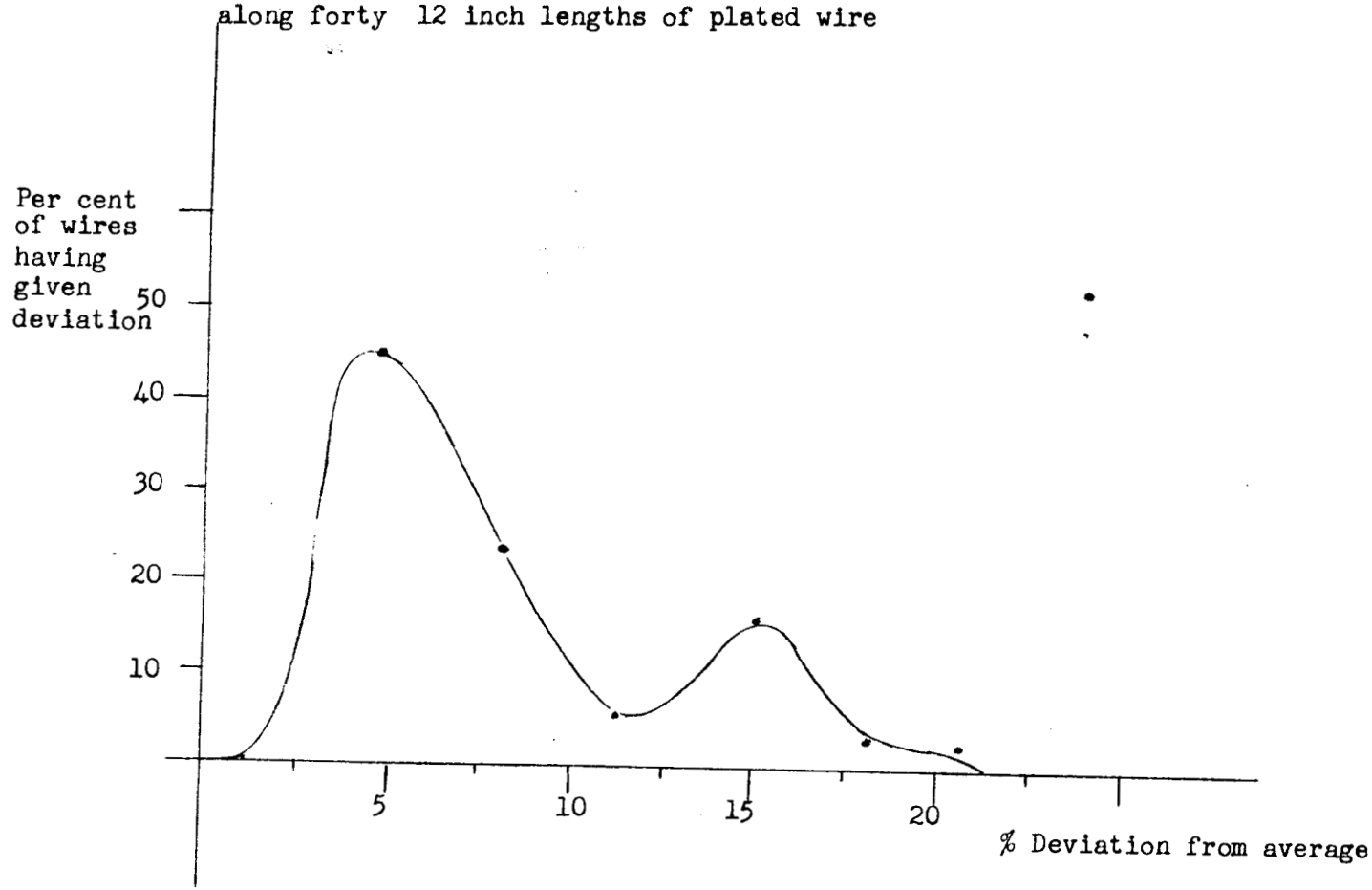


Figure 2.2.1

Data grouped in ±1.6% deviation intervals.

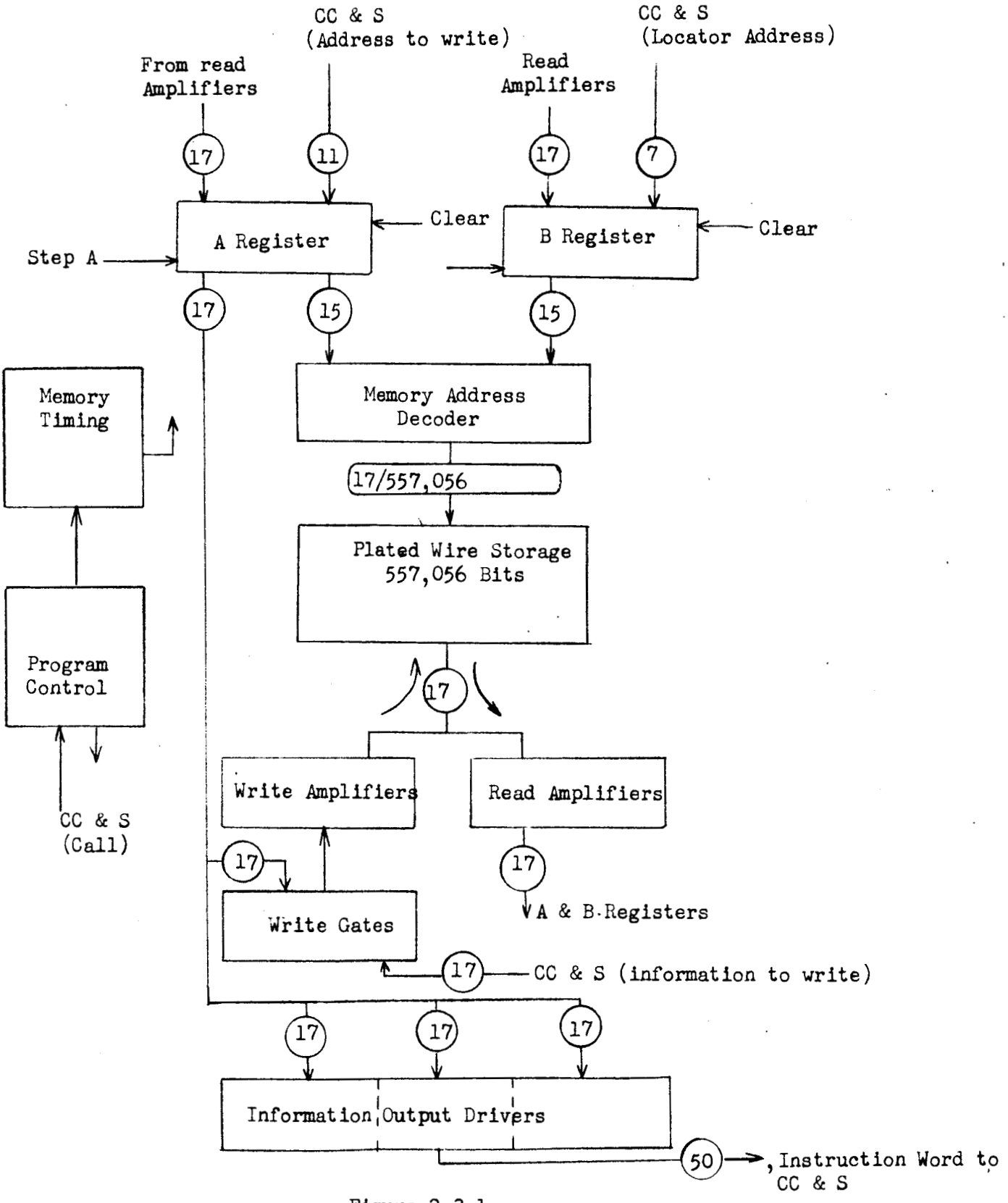

CC & S
(Address to write)
CC & S
(Locator Address)
From read
Amplifiers
Read
Amplifiers
17
11
17
7
A Register
Clear
B Register
Clear
Step A
17
15
15
Memory
Timing
Memory Address
Decoder
17/557,056
Plated Wire Storage
557,056 Bits
Program
Control
17
Write Amplifiers
Read Amplifiers
CC & S
(Call)
17
17
Write Gates
A & B Registers
17
CC & S (information to write)
17
17
17
Information Output Drivers
50
Instruction Word to
CC & S

Figure 2.3.1

LOCATOR STORE

128 locations x 17 bits = 2176 bits

MASTER PROGRAM STORE

128 programs x 20 words / program x
17 bits/word = 43,520 bits

SUB-PROGRAM STORE

500 sub-programs x 20 instructions/sub-
program x 51 bits/instruction = 510,000 bits

FIGURE 2.3.2

Proposed Programmed Memory Logical Flow Chart

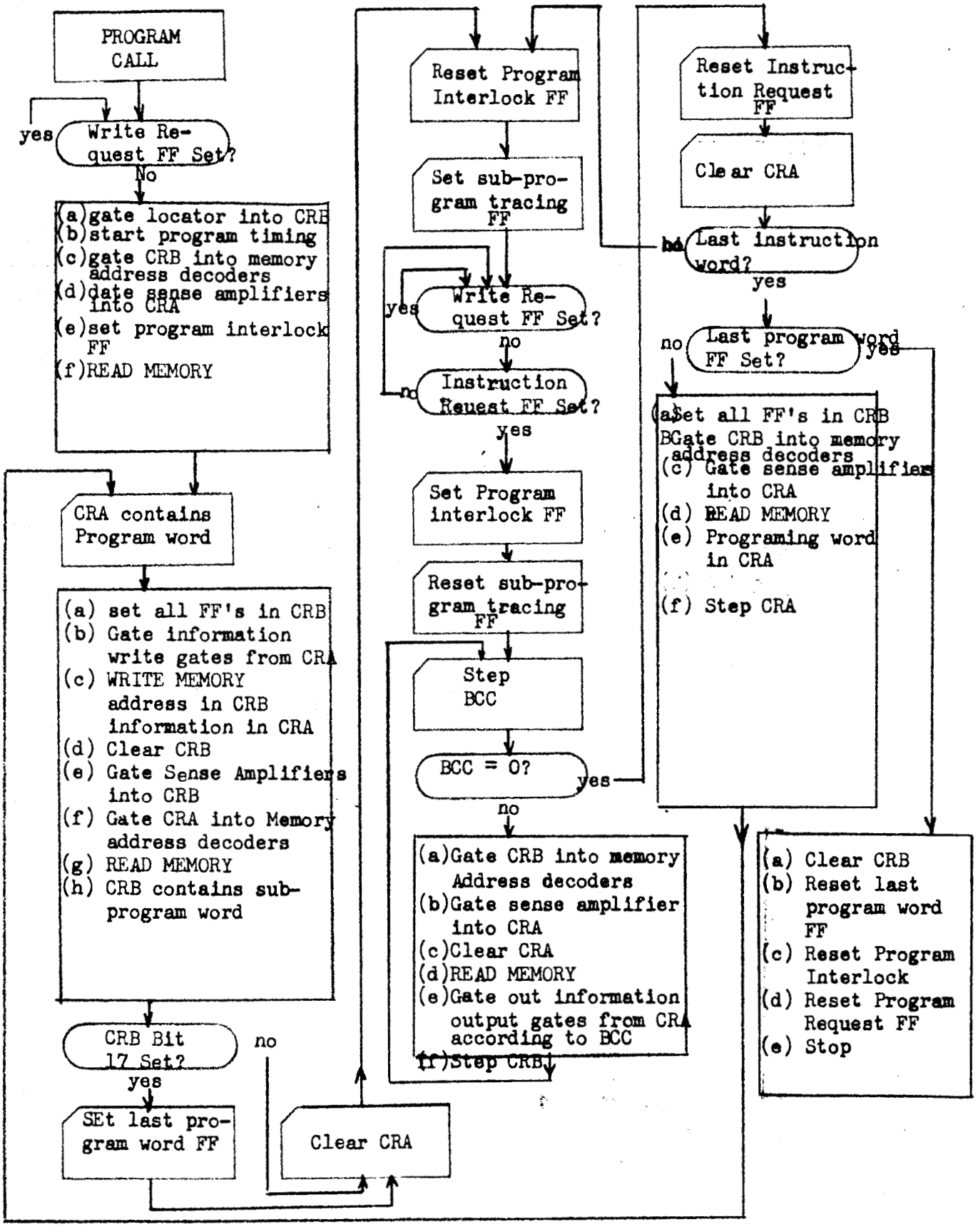


Figure 2.3.3 a

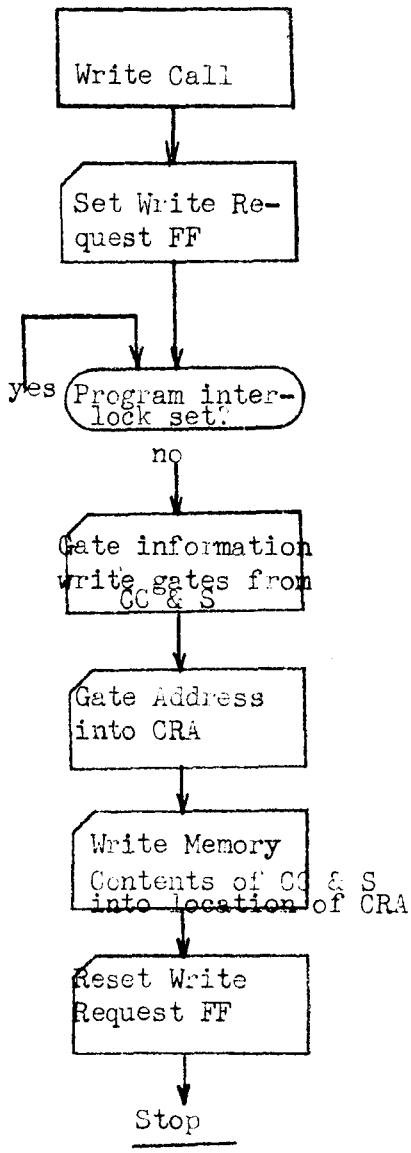


FIGURE 2.3.3b

Proposed Programmed Memory Logical Flow Chart
(write)

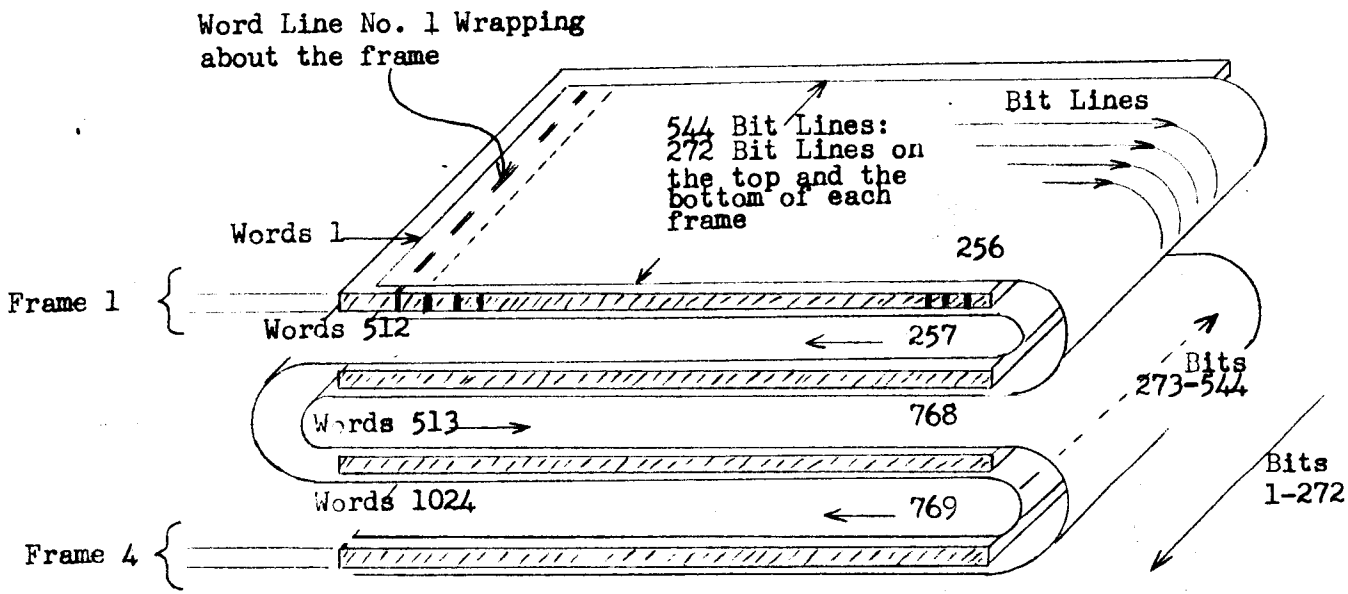


FIGURE 2.3.4

Location of Word Lines and Bits Among
The Four Frames of Stack Assembly

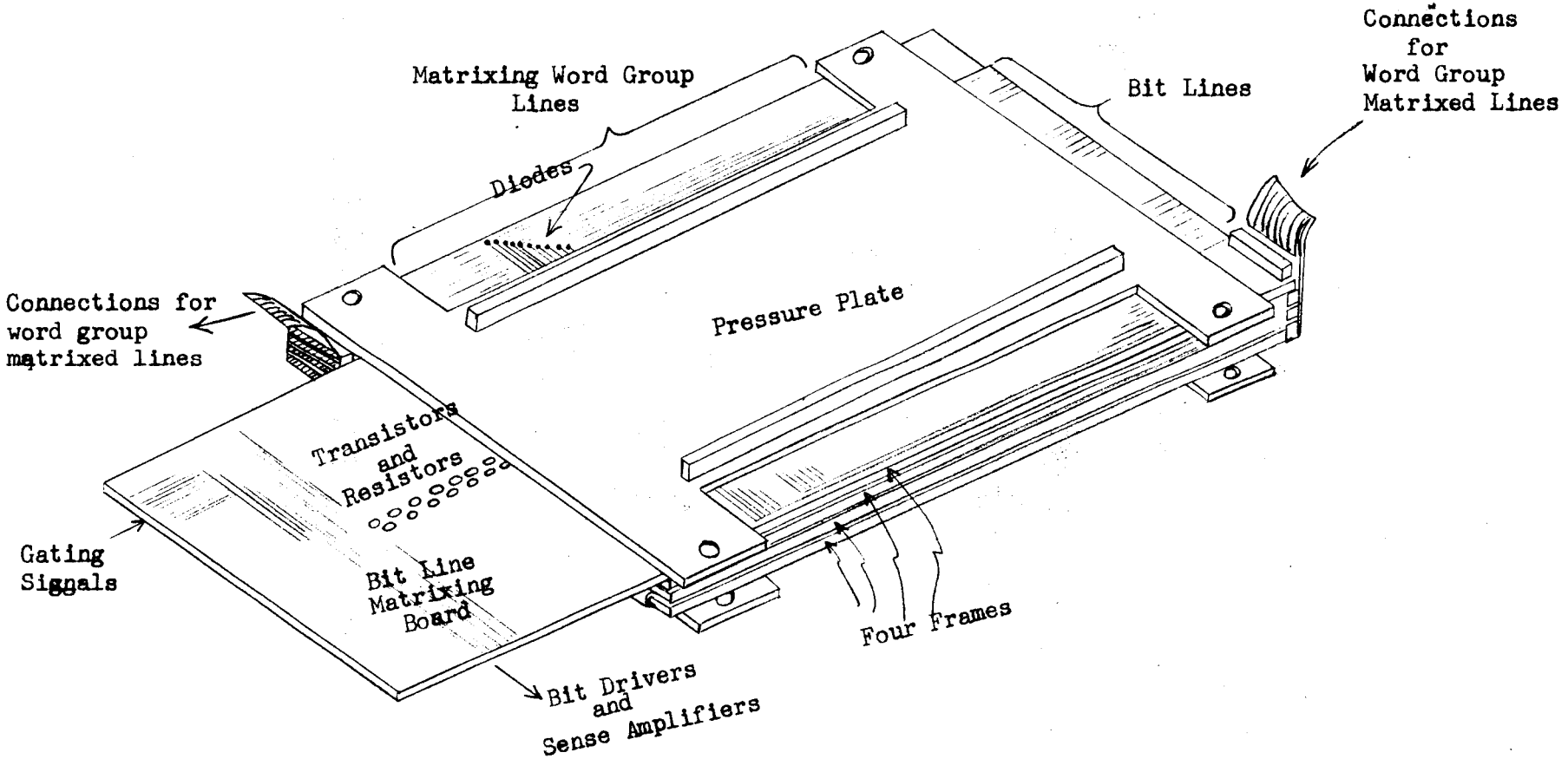


FIGURE 2.3.5

A Sketch of the Memory Stack Assembly

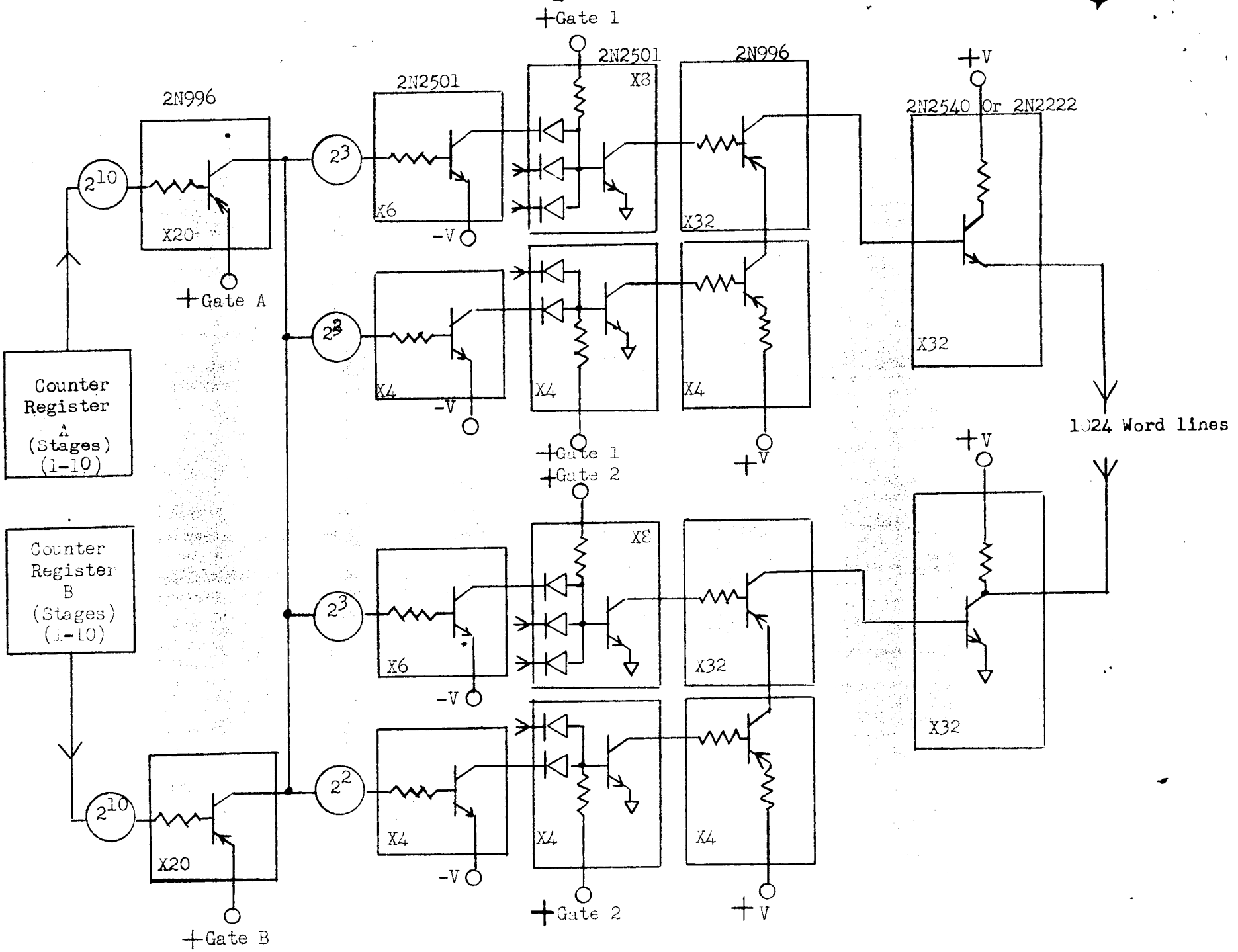


FIGURE 2.3.6
WORD LINE MATRIX AND DRIVERS

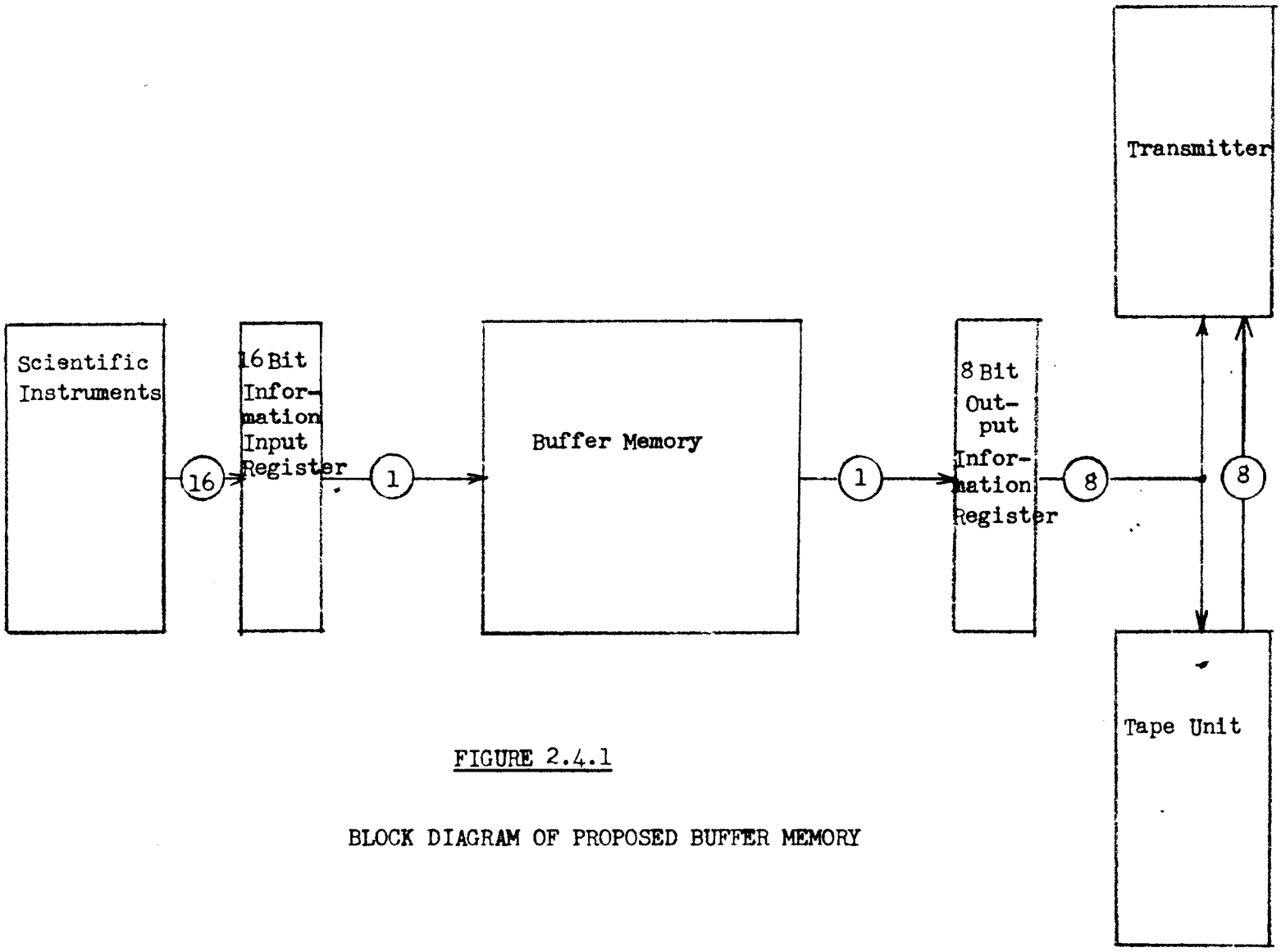


FIGURE 2.4.1

BLOCK DIAGRAM OF PROPOSED BUFFER MEMORY

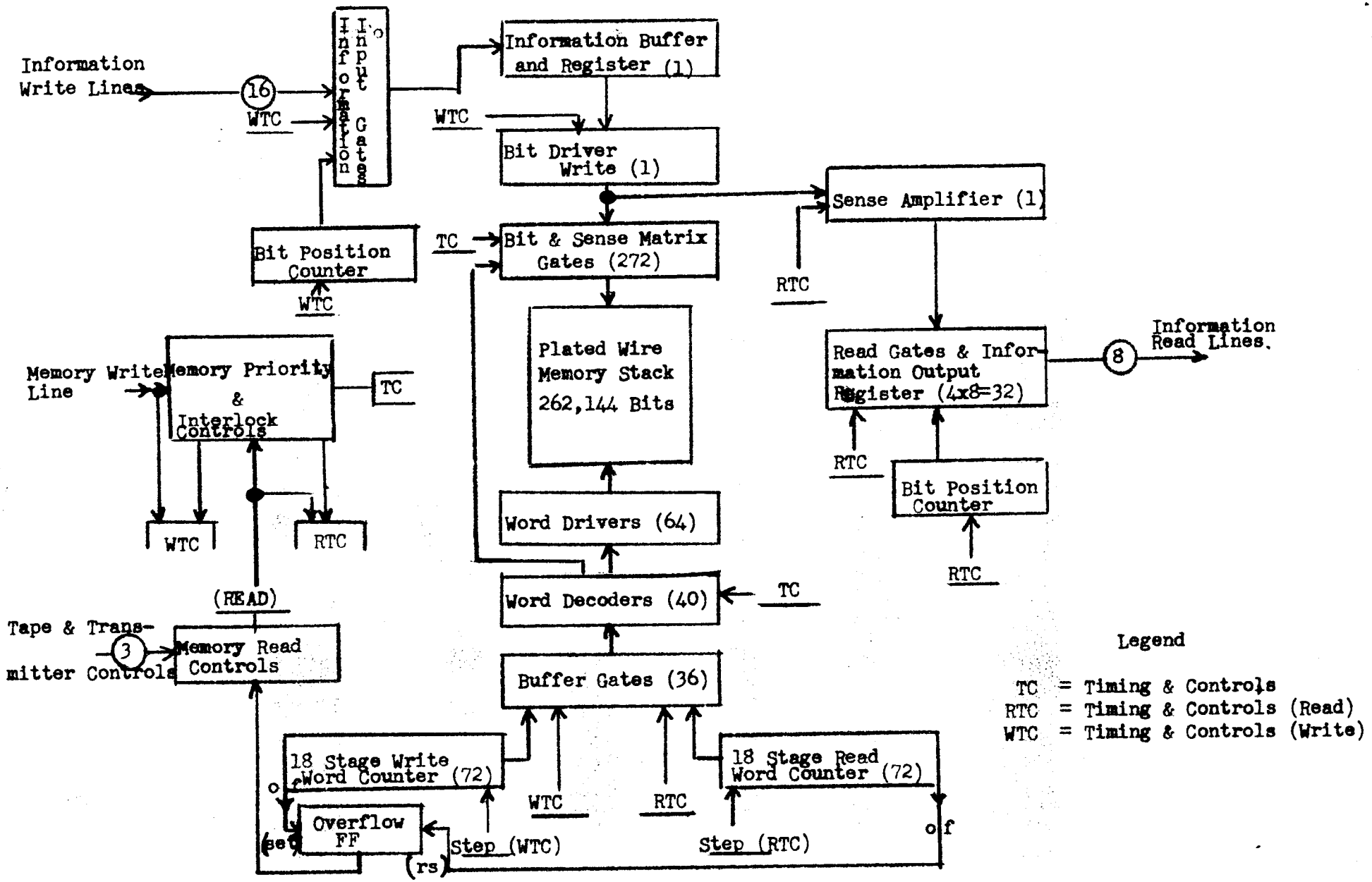


FIGURE 2.4.2

Logical Block Diagram of Proposed Buffer Memory

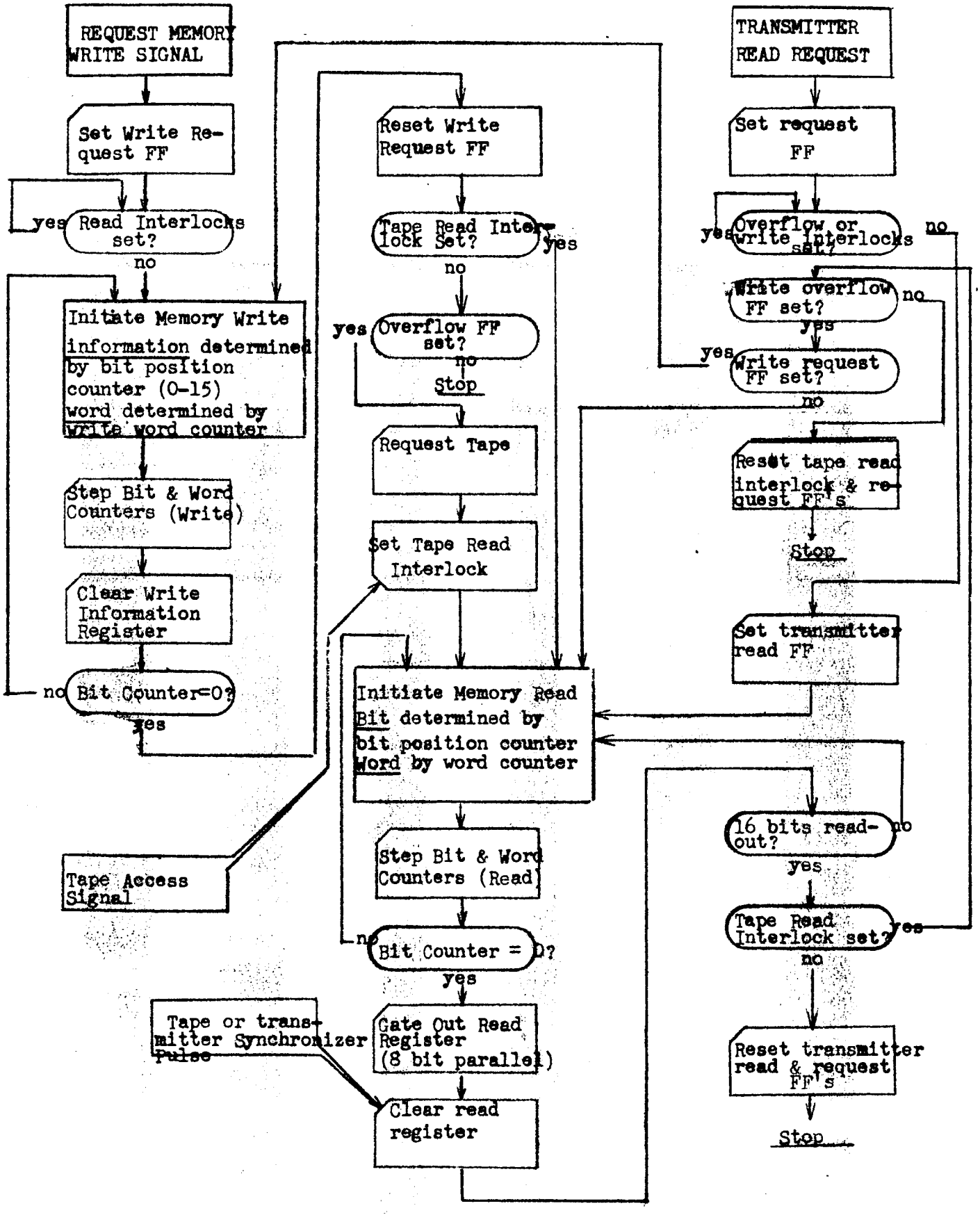


FIGURE 2.4.3

Logical Flow-Chart of Proposed Buffer Memory

3.0 CONCLUSIONS

1. Thin magnetic films have the necessary mechanical integrity for spacecraft application. The Curie temperature is so high, approximately 600°C, that other considerations will limit the operating temperature range. Magnetic films are manufactured with zero magnetostriction coefficient so that necessary protection against shock and vibration during operation is reduced.

2. As shown in Section 2.1 of this report, a reduction in plating thickness from 10,000 Å to 5,000 Å will reduce the required drive by nearly two-to-one. Past experience indicates that the switching time will also be reduced so that the peak voltage of the output signal will not be reduced proportionately to the volt-seconds. In addition, plating on smaller diameter wire will permit increased bit packing density, lower drive power with no loss of output for a given width of word line. These two items, plating thickness and wire diameter, offer very attractive approaches for developing a memory element whose properties are optimized for spacecraft applications.

3. The plated wire memory element has the following advantages that relate directly to spacecraft memory systems applications:

a. Nondestructive readout

b. Non-volatile, storage

c. Simple "write-in" mode. It is possible to write new information into one or many bits on a word line without disturbing the remaining bits.

d. Very low bit current drive and modest readout current drive.

e. Very low drive power because the induced back voltage on the readout line is small, and the drive current duration is very short.

f. The bit packing density is very high, approximately 800 bits per square inch of memory plane which is 1/8 inch thick including support, circuits and connections.

4. The power associated with driving the word and bit currents in the memory stack is almost negligible in comparison with the power consumed in the logic and sense amplifiers circuits. This is true because "D.C. level" logic is used instead of a pulse logic that uses power only to transmit information. Reduction of word line drive current is significant only in terms of the peak current capability of the drivers.

5. The thin magnetic film plated wire memory element cannot be used to fulfill a memory requirement of 10^8 or 10^9 bits in the next 3 to 5 years. Optimistic estimates of production cost of such a memory are in the 5 cents per bit range. Depending on the exact situation the upper size limit is probably around 10^7 bits because of the cost factor. These cost estimates were not make with precision and details have therefore not been included in this report. It seems highly improbable that any all electronic, completely random accessible memory can be used in a 10^8 or 10^9 bit memory in the next 3 to 5 years. The use of mechanical

motion to place new information storage media at write and read stations provides a cost advantage that may never be overcome by any electronic random access memory.

3.1 Recommendations

1. Continue the development of the plated wire memory element to optimize its operating margins.

2. Develop a smaller diameter wire substrate, perhaps 2 to 2.5 mils with a thinner plating of 5000 Å or less. This will permit higher bit packing density and reduce the drive current for possible compatibility with integrated circuits.

3. Develop logic circuits, registers, and matrix switches needed for the type of memory described in Section 2. Specifically, circuits that have a minimum or zero standby power with adequate noise protection. Based on experience with large scale very fast computer systems the 3 volt logic signals assumed in this report are very conservative and it seems possible to use a smaller signal voltage. Develop a switch core matrix with adequate rise time in its output drive current to make a definitive comparison to the diode word line selection matrix.

4. Combine items 1, 2, and 3 in a 1 year engineering development program that will result in a feasibility model. This model should demonstrate that a one half million bit memory can be operated at a 100 KC serial bit rate with 260 milliwatts. A full size memory stack should be built with a portion of the bits and circuits operating to demonstrate the size of 210 cubic inches. and weight of 9.2 pounds. The random access, in-flight writing, and non-volatile storage and non-destructive readout make it very attractive for future spacecraft application.